

## Scott Hopkinson









# **Personal Computer Design Guide:**

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## **A Survey of Integrated Solutions**

*Scott Hopkinson*

*Annabooks*

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by

**Scott Hopkinson**

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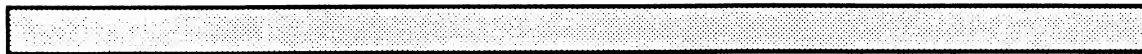


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## *Chapter 1: Introduction*

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During the compilation of this book, we discovered that the best reason for writing this book is due to the sheer number of alternatives available to the designer when developing a PC-compatible system. Who, as a design engineer, hasn't pored through the IC Master, EDN microprocessor survey, and various periodical sources for a preliminary selection of an integrated circuit or microprocessor?

When we undertook the task of putting together the available data on integrated personal computer chip sets, the size of the job blossomed into more than we had anticipated. The number of manufacturers in this market has been constantly expanding since companies such as Chips and Technologies not only entered the market but created it.

The market has evolved from this established base in two distinct directions. Initially, the first benchmark established in the market was the integrated peripheral controller. Looking at the original IBM PC/AT design, these integrated controllers included emulations of the Intel 8237 DMA controller, 8259 interrupt controller, DMA address extension, and refresh logic. This design is characterized by the Chips and Technologies' 82C206 product. There are no less than ten alternate, pin-compatible parts. The other direction of the evolution of this market has been the vendors that have been introducing a stream of products. These have continually added architectural features such as ROM BIOS shadowing, power-down control, efficient utilization of memory bandwidth, cache memory, and additional peripheral functions such as IDE disk support, additional communication lines, and parallel ports.

Added to all this, the semi-custom circuit vendors have been anxious to participate in the burgeoning market of PC-compatibles. By adding the standard Intel peripherals to their macro-function library, their customers, the OEM system houses, can build their own chip sets. Taking this approach allows the vendor both to have better control of their destiny of computer design and to develop system architectural features that allow for product differentiation.

### *Survey Methodologies*

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The selection decision for engineers must include issues of time to market, cost, product differentiation, and future migration. Some aspects of this strategy must include plans for migration of the design with emerging technology.

The purpose of this book is to provide a source for beginning the selection criteria of any PC-compatible system design. These systems can take the form of either a typical desk-top system or a personal computer embedded in an application.

In order to facilitate the location of information in the survey section of this book, we have organized a summary section that will point the reader toward a more detailed description of the chip sets that may be useful for the application. The detailed data sheets are organized by manufacturer rather than by type of machine.

### *History of PC Chip Sets and Architecture*

---

George Santayana observed in his book *Life of Reason*, "Those who cannot remember the past are doomed to repeat it." Like those who study history, we are compelled to look back at the evolution of the PC chip set development to appreciate the design and system considerations that have been addressed by succeeding integrated solutions.

The changing factors that affect the succeeding generations of solutions are not only the levels of integration which are possible, but such mundane subjects as packaging technology and low-cost manufacturability. The cost of building a board that utilizes surface mount devices and lead spacing of 25 mils would have been considered prohibitive in the early 1980s, and yet are now the order of the day.

Looking back over the past fourteen years, the personal computer timeline, shown on the next page, shows an ever-increasing level of integration and computing power. Personal computers have allowed people to discover new possibilities for applications that were not considered possible before the computing technology was present to support it. Today, the graphical user interface is a standard that most users expect of their systems; but not until recently have these systems been capable of supporting the resolution, display density, and screen update performance demands for such a system. Multi-media now promises to create yet another opportunity for expansion of the application base for which personal computers will find new uses.

These changing requirements for performance will, in turn, have an effect on the development of various components of the computer system. The graphic user interface coupled with the ever-increasing capability of putting logic functions on a semi-custom logic device have combined to create an opportunity for the acceleration of the graphical interface.

1978	8086 processor introduced
1979	8088 processor introduced
1981 August	Original IBM PC introduced (5 MHz 8088)
1982	80286 processor (16 MByte address space)
1983 March	PC/XT introduced
1984 August	PC/AT introduced (6 MHz 80286)
1984 June	Compaq System Pro introduced (based on 8086)
1985	80386DX processor introduced (32 bit data, 4 GBytes address)
1986 April	PC/AT 8 MHz introduced
1987 July	PC/AT dropped by IBM
1987 July	PS/2 line introduced by IBM
1988	80386SX processor introduced
1989	80486DX processor introduced
1991	Accelerated graphics integrated solutions introduced
1991	80386 clones enter the market
1991	80486SX processor introduced
1991	Multi-media begins to gain attention of developers
1992	80486 double-clocked processor introduced
1992	Local bus gains interest. Two competing standards: VL and PCI
1993	Successor to '486 introduced (Pentium / P5 / '586)
1993	16 MBit memories begin shipping

***Table 1.1: Personal Computer History Timeline***

The PC/XT system structure, shown in Figure 1.1, represents the original foray of IBM into the desk-top computer marketplace. Up to that date, "real" computers were either mainframes or mini-computers. Mini-computers represented a revolution for the computer industry that eventually gave way to the personal computer. With the advent of the mini-computer, the concept of the user directly communicating with the computer came into reality. With the typical mainframe installation, the normal manner of accomplishing work was to submit a program (or "job") to the system and direct the results to a printer or other output device for later analysis. Software development meant that the programmer would be lucky to get three to four compilation runs in each day.

Mini-computers were not only much more cost-effective and smaller, they brought about the idea of interactive computing. The user was directly connected to the system, typically using an ASCII terminal as an asynchronous communication line. The user could then expect to accomplish considerably more with the system in a day. This, of course, brought the computer closer to the human interface and put the additional requirement of that additional computing task on the system. That direction in computing hasn't changed and doesn't appear likely to in the foreseeable future.

There were several advantages of the mainframe and mini-computer style of computing models that the personal computer revolution lost out on until networking began to come into play. Among the advantages of centralized computing resources were the system administration tasks of back-up, and keeping data that is shared by multiple users up-to-date. In a mini-computer or mainframe, it was a natural phenomena that programs and data structures that were shared by multiple users were available to those users in a shared file structure system. With a computer in front of each user, each with their own disk, this was not such a natural way of using and sharing data.

Another aspect of the centralized computer environment was that this computing resource (the CPU , Memory, Cache and System I/O) was available to be brought to bear on whatever task was currently running on the system. This meant that a computer that was only two or three times more powerful than an individual computer system would "appear" to be faster to several users. One major reason for this was that the typical user's programs would spend 99 % or more of the time waiting for the human to interact with or respond to the computer. Users definitely have a perception that their time is being wasted if, when entering the last data item in a large spread-sheet, the computer takes more than a few seconds to re-calculate all the data items in the spread-sheet; however, in a shared computing environment, the demand for re-calculation is statistically spread over time, so when one user is re-calculating a spread-sheet or waiting for a compile the other users are typically entering data and don't notice that they are only getting 2 % of the system's computing power for running the editor session.

Personal computers have moved us in the direction of a more distributed computing model to allow the individual users "freedom" to accomplish tasks that would otherwise not be feasible or at the least require justification for the "Computer Services" department of the traditional centralized computing model.

### ***Personal Computer Architecture Evolution***

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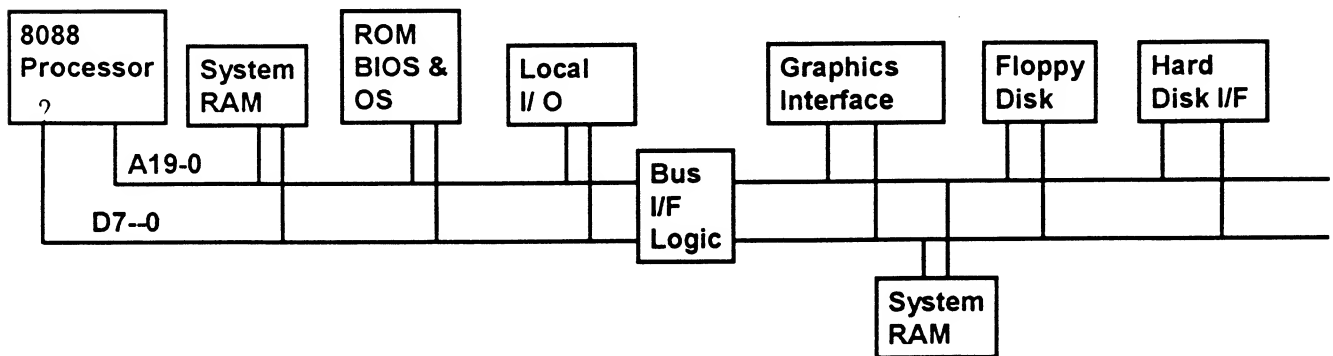
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Personal computer architecture has evolved over the years as demands of different parts of the system have grown and the users have become more sophisticated in their expectations of what the computer system can do. Many of the architectural changes that have been introduced in the growth of the computers have come from the mini-computer and mainframe designs of the past. Some have evolved only recently with the advances of semiconductor technology. Some of these architectural developments are discussed in this section.



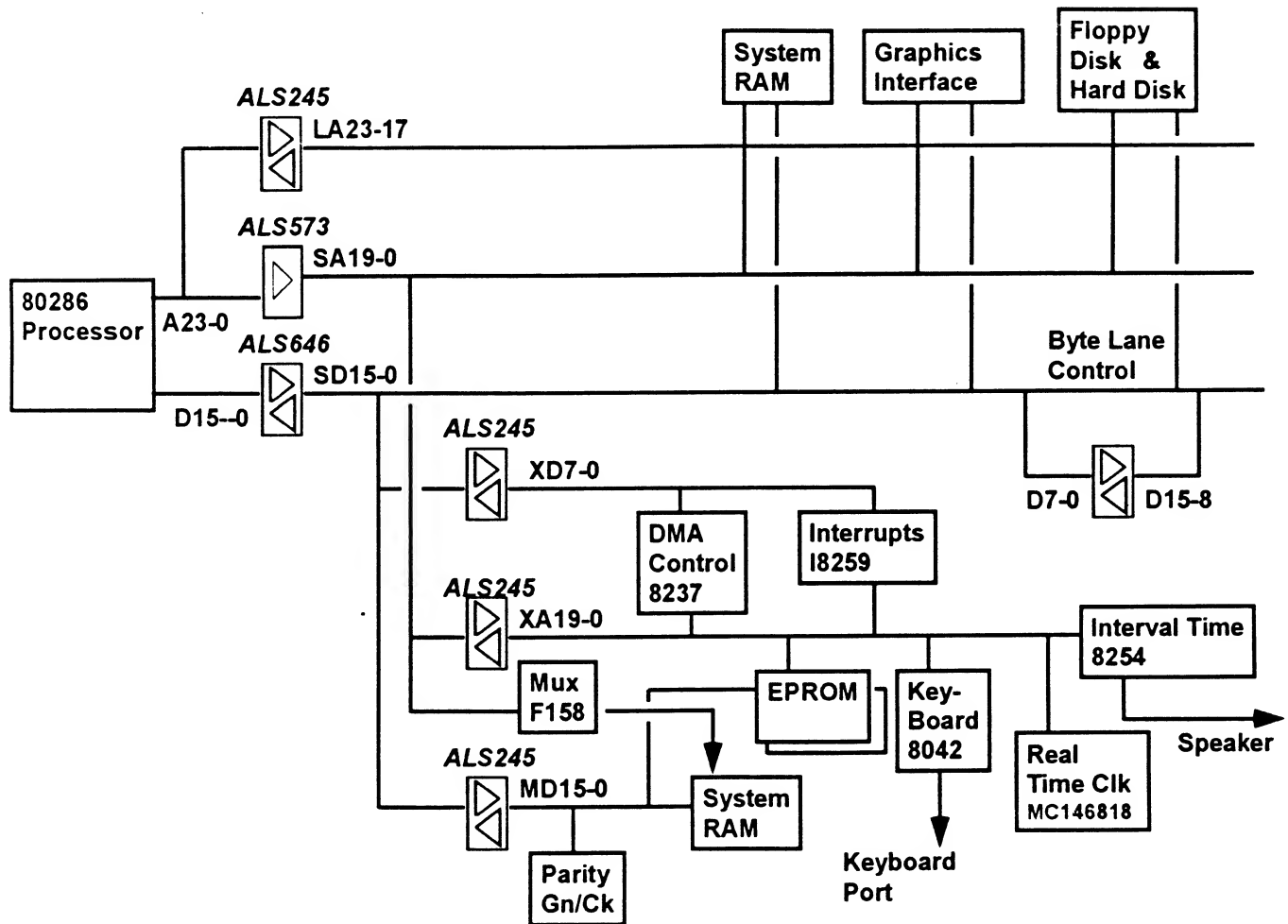
First, however, let's make a quick review of the first two IBM personal computer architectures, followed by a summary review of some of the more recent developments and how they have affected the standard PC architecture.

The following block diagram shows the structure of the PC and PC/XT system. Looking at the system from a bus structure viewpoint, the system tied all the components to the same "logical" bus. The processor was separated from most of the other system components by a set of bus transceivers, but the system fundamentally tied all the components together. When the DMA function was active, the processor was stopped. This machine was designed to execute from its ROM-resident operating system and even included a tape interface for users that did not have a floppy disk interface to the system. IBM included with this system a BASIC language interpreter in ROM so that the users could immediately have access to a programming language.



**Figure 1.1: Original PC/XT Block Diagram**

Several years later, IBM introduced the PC/AT . This system design, shown in Figure 1.2, attempted to retain some level of backward compatibility with the XT in several areas. First, add-in cards designed for the XT would plug into the AT platform. The system bus was designed to be a dynamic, self-sizing bus that would detect if a slave device card responding to a memory or I/O operation was a sixteen bit or eight bit card. This backward compatibility goal led to several other design decisions that were part of the AT and continue to be a part of most "compatible" machines today.



*Figure 1.2: Original PC/AT Block Diagram*

Several aspects of the AT platform design were driven directly by the desire to maintain backward compatibility with the XT. Some of these design goals are described in the following sections.

### *AT/XT DMA Compatibility*

To maintain backward compatibility with the XT, the designers of the sixteen bit AT platform elected to add a second DMA controller in the system with the specific responsibility for sixteen bit transfers. In order to maintain backward compatibility with the XT, this DMA controller, implemented with the Intel 8237 DMA controller circuit, was "cascaded" from the first controller and set up to generate sixteen bit addresses instead of eight bit addresses.

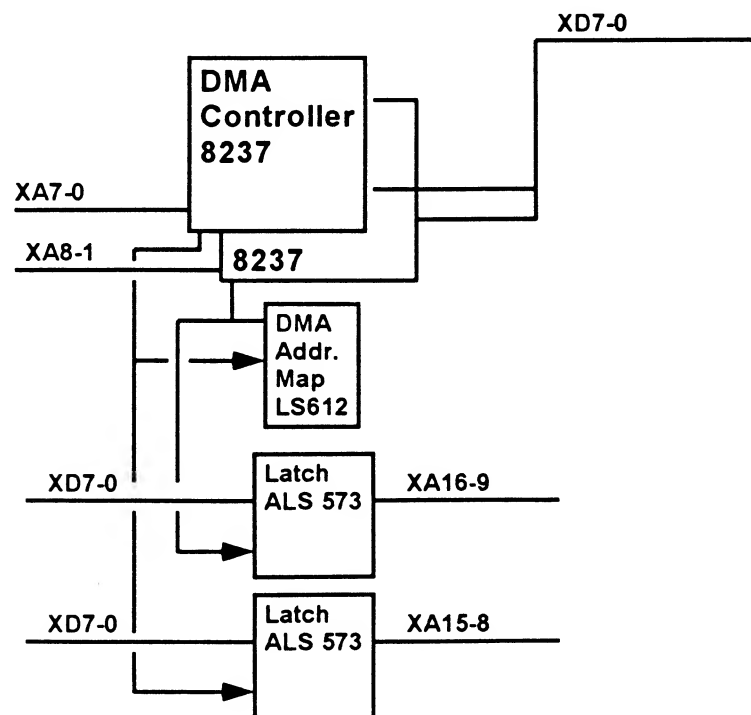
The 8237 DMA controller was designed as a byte-oriented controller that would simultaneously read memory and write to an I/O location or, alternatively, read an I/O location and write to a memory location. Its normal manner of being used in a PC is accessing a fixed I/O address and writing to or reading from ascending addresses in system memory. Referring to the block diagram, the reader will notice that the DMA controller requires external logic to hold the "upper" address bits (A15 to A8) to the system. In order to allow the DMA controller to address sixteen bit words instead of bytes, the address connection from the second (AT) DMA controller were "offset" by one bit and so instead of directly driving A7 to A0 and through a latch driving A15 to A8, the sixteen bit DMA controller of an AT drives directly the A8 to A1 bits and the A16 to A9 bits through a latch.

The PC/AT also had the capability of addressing more than the one megabyte address space of the original XT. To support this additional addressing range, the AT design included a simple address mapping / extension mechanism for the DMA controller. This "map" was originally implemented with a 74LS670 type register file. Each entry in the register file held the upper address bits for the given DMA transfer. This "map" had to be reloaded from the processor in order for the DMA to cross a 64K byte boundary for eight bit DMA, and a 128K boundary for sixteen bit DMA. EISA systems had to extend this concept even further to allow the addressing across the full thirty-two bit address range defined by EISA. In all these systems, backward compatibility with the original PC/XT and AT DMA controller has been maintained.

To maintain compatibility with both XT and PC/AT systems, EISA again extended the addressing for DMA operations. The basic 8237 DMA controller supported sixteen bits of addressing. These were used for address bits fifteen through zero on the DMA controller associated with eight bit transfers, and sixteen through one on the "cascaded" DMA controller that was added for PC/AT and sixteen bit DMA. Beyond that, as described above, the PC/AT used an eight bit wide mapping register (implemented with 74LS612s) to extend the address to twenty-four bits. EISA added to this scheme with an additional set of address mapping registers that add an additional eight bits to the effective address and create a full thirty-two bit address.

In addition to this mapping, EISA also added the mechanism of Buffer Chaining. Basically, the buffer chaining definition of EISA allows the driver software to set up the next segment of the DMA transfer while the current transfer is taking place. When the DMA controller reaches the end of the current transfer, the new address, mapping address, and byte counts are loaded into the DMA controller and the DMA begins to proceed at the new address immediately without delay or intervention. During this next DMA transfer, the processor can then update the next address, address mapping, and byte counter registers.

One of the other issues involving the DMA of the original PC platform is the latency of the DMA channel. Unfortunately, the approach of "cascading" the second DMA controller (for sixteen bit transfers) off of the eight bit DMA controller for compatibility has the side effect of creating an excessive delay for DMA arbitration. This latency is on the order of 1.5 to 2.5 microseconds for the controllers. Early DMA-capable board level products quickly ran into that limitation for transfer on the system bus. Since this latency was so long relative to the potential cycle time of the bus (about 0.3 microseconds) the realizable bandwidth for DMA was nothing near the bandwidth the processor had for accessing the system memory nor was DMA nearly as fast as it could have been. More recently, DMA controller cards have been developed that have internal FIFO memory that can queue up a number of transfers while waiting for the arbitration delay of the bus. When the DMA controller is granted access to the bus, the controller can transfer a number of words and thus distribute the arbitration delay penalty across multiple transfers.



*Figure 1.3: AT DMA Controller Address / Data Path*

## First Levels of Integration

The first company to recognize the emerging compatibility marketplace and the opportunity for higher levels of integration was Chips and Technologies. One of their early offerings is shown in Figure 1.4.

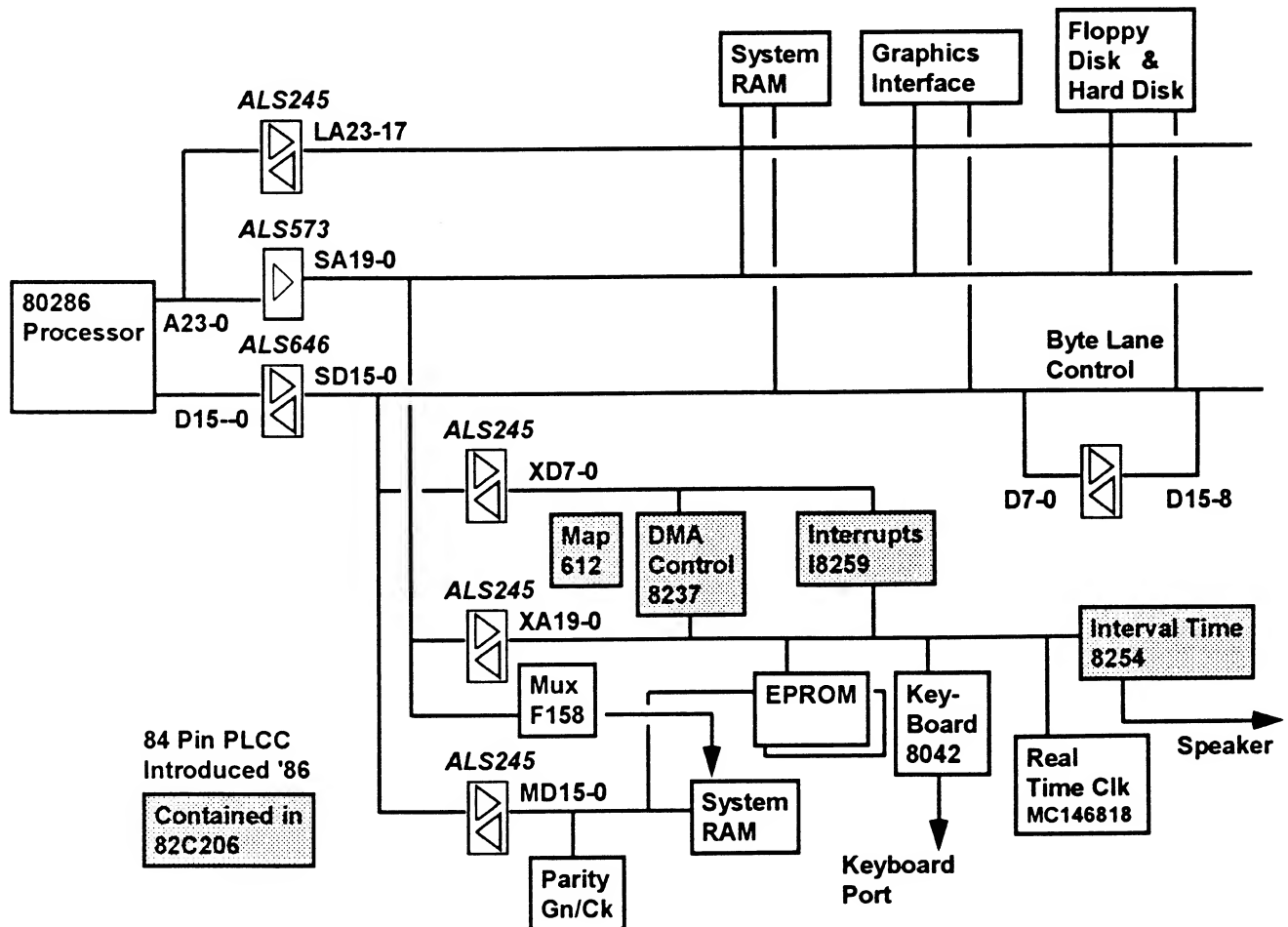


Figure 1.4: Chips and Technologies AT Chip Solution

## *Other Architectural Trends*

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In the last few years, the emerging lap-top and notebook computer market has given rise to an even more integrated solution. To complicate the design effort for these products, the engineers also are forced to consider the power consumption issues.

CMOS technology has gone a long way to improve this aspect of computer design. CMOS logic uses a structure (Complementary, Metal Oxide Semiconductor) that consumes power mostly during switching. Since the transistors of CMOS logic are MOS FETs, there is very little leakage current from the gate to the source or drain when the transistor is not switching. However, when the device starts switching, the power consumption goes up as a function of the frequency at which it switches.

First generation integrated solutions from Chips and Technologies used bipolar buffers for the bus interface drivers to provide the specified 24 mA drive necessary to meet the de facto PC/AT bus standard established by IBM. This bus is generally an asynchronous bus, with some timing tied to the bus clock signal (BCLK) that uses low power Schottky to drive and receive signals on the bus. This standard has lived and propagated to the EISA bus, which extends the address and data paths to thirty-two bits and provides for faster bus cycles than the fastest of the PC/AT (also known as ISA) bus. Both the EISA and PC/AT bus use the "LS-TTL" drive specification of 24 mA sink and four micro-amps source with the classical TTL threshold logic levels of 0.8 Volts and 1.5 Volts.

## *Personal Computer Bus Strategies*

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The PC/AT bus was developed as a natural extension of the Intel processor that was first used in the PC/XT system. From that eight bit I/O channel, a sixteen bit variant was designed to provide backward compatibility with cards designed for the eight bit channel. The EISA bus continued this backward compatible capability by allowing either PC or PC/AT cards to be inserted and used in the EISA connector. The EISA bus protocol allows the system to determine, through the EISA configuration mechanism and the bus protocol, if the card attached is an EISA or PC/AT (ISA) or PC/XT card.

The PC/AT channel is capable of transferring about eight megabytes of data per second when accessing system memory and utilizing the zero-wait-state feature of that bus. Disk controllers originally used on this system relied on a simple, non-DMA disk controller for movement of data.

Most busses have performance advantages with the use of DMA instead of programmed transfer, but the AT bus is an exception to this rule. When DMA is performed utilizing the Intel 8237 DMA controllers in the system, a severe performance penalty occurs. This is due to the design of the original IBM PC/AT and its backward compatibility with the PC and PC/XT. The DMA controller in the PC/AT was "cascaded" from one of the DMA channels in the XT architecture in such a way that the sixteen bit DMA transfers supported by the AT required that the DMA controller (Intel 8237) had to arbitrate using the eight bit DMA controller.

Because of this "cascading" of DMA controllers, the latency of acquiring the bus takes a long time and lowers the performance of the DMA device on the bus. Developers of PC-compatible chip sets were very concerned about maintaining compatibility with the existing designs at the software and hardware level. This aspect of successfully marketing a chip set was so important that developers of the chip sets went to great lengths to verify that any unintentional error or mode of operation introduced in the PC/AT design was duplicated in the chip sets for building clones. The design criteria requiring that the chip set matched exactly the operation of the original design was a much more dominant design consideration than those of performance. Only in the last few years has the issue of performance begun to have an effect on design considerations.

The following table shows the relative bandwidth performance requirement of various peripherals that are found on a typical PC clone. It is interesting to contrast these bandwidth requirements with the available bandwidth of the various busses.



Bus	Type of Access	Bandwidth	Base Clock
AT	Memory Access One Wait State	4.0 MByte/sec	6.0 MHz
AT	Memory Access Two Wait State	1.5 MByte/sec	6.0 MHz
AT	Memory Access One Wait State	5.3 MByte/sec	8.0 MHz
AT	Memory Access Two Wait State	2.0 MByte/sec	8.0 MHz
AT	Programmed I/O	2.2 MByte/sec	6.0 MHz
AT	Programmed I/O	2.9 MByte/sec	8.0 MHz
EISA	Memory Access Burst	33 MByte/sec	8.33 MHz
EISA	Memory Access Average	24 MByte/sec	8.33 MHz
EISA	DMA Compatible	2 MByte/sec	8.33 MHz
EISA	DMA Type A 16 bit	2.6 MByte/sec	8.33 MHz
EISA	DMA Type A 32 bit	5.3 MByte/sec	8.33 MHz
EISA	DMA Type B 16 bit	4.0 MByte/sec	8.33 MHz
EISA	DMA Type B 32 bit	8.0 MByte/sec	8.33 MHz
EISA	DMA Type C 16 Bit	16.6 MByte/sec	8.33 MHz
EISA	DMA Type C 32 Bit	33.0 MByte/sec	8.33 MHz
DRAM Bank	32 Bit Page Mode *	44 MByte/sec	33 MHz
VL Local Bus	32 Bit Access	66 MByte/sec	33 MHz
PCI Local Bus	32 Bit Access	120 MByte/sec	33 MHz
'486 local bus	32 Bit Memory Access Burst **	133 MByte/sec	50 MHz
Next Generation	Memory Access Burst ***	300+ MByte/sec	

\* : 180 nsec initial cycle plus 3 cycles at 60 nsec = 360 nsec/ four words (16 bytes)  
11.1 MXfers/Sec = 44 MByte/sec.

\*\* : 50 MHz, 6 cycles to generate address and read four word burst.

\*\*\* : Estimate.

**Table 1.2: Current Bus Bandwidth Capability**

Device	Bandwidth KBytes/sec Max Rate	Bandwidth KBytes/sec Average Rate
Keyboard	0.01	0.01
Mouse	0.02	0.02
Voice Input	0.02	0.02
Network-Terminal	0.05	0.05
Voice Output	0.60	0.60
Line Printer	1.00	1.00
Laser Printer	100.0	100.0
Scanner	200.0	200.0
Network-Ethernet / 10BaseT	125.0	125.0
Network-Token Ring	250.0	250.0
Display Buffer	200.0	200.0
Optical Disk	500.0	500.0
Magnetic Tape	1,500.0	1,500.0*
Magnetic Disk (slow)	930.0	186.0
Magnetic Disk (3.5 Inch high perf.)	3,500.0	600.0
Magnetic Disk (Fast/Large)	6,500.0	812.5

\* while tape is streaming, during backup

**Table 1.3: System Devices and Typical Bandwidth Requirements**

Some of the above transfer rate numbers deserve closer examination. How is it that a disk with a transfer rate of 3.5 MByte/sec (28 million bits per second) at the head only produces an average transfer rate of 600 KBytes per second average transfer rate? The mechanical nature of rotating storage becomes a dominant factor in performance for the typical transfer to and from a disk.

The typical disk request is four kilobytes (4,096 bytes) in length. Some operating systems and environments, such as Novell and UNIX, have stretched this request length to eight or sixteen kilobytes. Between each of those transfers, the disk must seek to the cylinder of the next requested data and wait for the rotational latency of the disk to begin the next read or write operation. A typical high performance disk is capable of seek times in the range of twelve milliseconds and a rotational latency of eight milliseconds. What results is that the average time required to transfer the average 4K block of data is on the order of twenty-two milliseconds (12 msec seek + 8 msec rotational + 1.5 msec data transfer). At this rate, the disk is capable of about 45 I/O operations per second, each of which transfers 4,096 bytes. This is how a 3.5 MByte disk results in an average transfer rate of 600 KBytes/sec.

Several factors have recently changed the performance issues for the personal computer. Beyond the processor performance increase, which allows users to process much more data, the use of windowing environments has significantly increased performance demands on the video interface. The original PC needed to manage communication with a screen that was 80 characters by 25 lines. This communication required only 2 KBytes to update the entire screen. State-of-the-art video displays now contain 256 KBytes or more of display memory (1 MByte is not unusual) and so the data rate required to update the screen in 1/10 of a second (near the boundary of human perception) has gone from 0.020 MByte /sec to 2.56 MByte/sec (over a hundred-fold increase).

This demand, driven on by Windows and other graphical user interfaces, has prompted system vendors and integrated circuit vendors to develop two strategies for improving performance to the display memory. First, the interface intelligence for the display sub-system has been improved with support of drivers and hardware for such fundamental functions as line draw, rectangle fill, and bit-block move. Secondly, the interface between the processor and the video subsystem has been moved to a point in the system where the transfer rate is no longer limited to the four or five megabytes per second of the ISA bus, but now can take advantage of transfer rates in excess of 100 MByte/sec.

Quick to follow that trend for higher-end systems will be locally-attached mass storage. Although performance gains are made with this closer attachment, the overall improvement will be significantly less than for video due the limiting bandwidth of the mechanical disk. Several vendors of network interface products have also indicated their intention to support local bus interfaces. Again, the basic transfer rate of an Ethernet interface does not benefit from the ten-fold increase in bus bandwidth.

Standard busses will continue to be present in systems, and with graphics and disk interfaces (mostly IDE) being supported within the core system logic. Many (or possibly most) systems will be adequately built with an ISA bus interface rather than the EISA higher-cost bus. The EISA market will still provide a very adequate I/O sub-system bus for servers and higher-end computers that have special (high performance), non-standard interface requirements.

The market-driven solution of increasing system performance outstripping the dated bus interfaces has been the migration of all the system elements on the one system bus to an architecture where first system memory and then video have moved closer to the processor and thus higher performance busses. In addition, items that were part of add-on cards but found on many, if not most, systems have been incorporated in standard peripheral support chips. A typical peripheral support circuit includes two serial ports, a parallel port, the floppy disk controller interface, and support to minimize the interface to the IDE (AT attachment)-type disk drive. Often this interface also supports a mouse interface as well. The typical system doesn't require

any additional peripherals to be a complete single-user system. For business applications, a network interface or modem interface can be added via the industry standard I/O slots. These two peripherals do not generally suffer from the performance of the ISA bus.

When you review the original PC/AT architecture block diagram in Figure 1.2, it is important to note that although there were several different major busses in the diagram, they were all logically tied to each other. Whenever an access was going on relative to the CPU, the system bus, memory bus, and local peripheral bus (xbus) were all being used, or at least restricted from being used. This trend continued with the increasing speeds of the Intel 80286, and many manufacturers attempted to sell motherboards or systems in which the ISA channel (AT bus) kept pace with faster processors. Most systems built around a ten or twelve megahertz bus clock either had severe compatibility problems or had to have a mode where the bus or the entire system could be brought back to the eight megahertz of the original system. With the advent of the thirty-two bit processor from Intel, this approach was rendered moot. Now the processor had the ability to consume data at twice the rate of the bus by virtue of the wider path to the processor.

In the spring of 1986, several companies got together and formed the PC/ET consortium for the purposes of defining a thirty-two bit extension to the PC/AT bus that was heretofore undocumented, except within IBM and several major clone manufacturers that had developed their own standard (or variation) of the original specification. The PC/ET activity was spearheaded by Phoenix Technologies and never successfully completed a specification that was implemented. Several working draft proposals were put forward for consideration, but none carried sufficient agreement and technical soundness to become a standard.

Out of that work, several organizations realized that there was a need for codification of the existing standard. It was the contention of these members of the early work that any bus based on a superset of the PC/AT bus, and sharing its signals, would be unable to keep up with the pace of processor development and the bandwidth requirements. At the same time, the need for a standardized general purpose I/O channel was evident and the ISA bus was adequate for most, if not all, of the peripherals in use on PC systems at that time. This was the beginning of the IEEE P-996 standardization activity.

At that time, video was character-based and disk transfer rates were typically about 625 KBytes/sec (5 Mbits/sec). In addition, the dominant disk controller on the marketplace was a three-to-one interleave controller giving a maximum average transfer rate of 208 KBytes/second. The ISA bus, with its two megabytes/second program move transfer capability and its six to eight megabytes/second bus master transfer rate was more than adequate for even the fastest disk of the day. Even today,

the fastest multi-gigabyte disks transfer data at a rate of seven megabytes per second (56 MBit/sec) only on the outer recording zones.

Today, however, three phenomena have caught up with the PC/AT or ISA bus. First, the processing speed (and thus the data transfer demand) of processors have been growing at an exponential rate. One industry leader in the RISC workstation market has predicted that the MIPS for a particular year can be given by the formula  $2^{*(YEAR - 1984)}$ . That translates into a growth rate from one MIP (million instructions per second) in 1984 to 64 MIPS in 1991. Although we are not exactly on that curve, the Intel 80486 DX2/66 approaches 24 MIPS and the Pentium is rumored to be twice that. The data rate that such a processor requires to feed its execution engine has actually increased faster than the computing rate due to speculative execution and cache line fills that are never used.

Secondly, the phenomena of a graphical user interface (also known as GUI) has significantly increased the demand on the video interface part of a system. Where it once was adequate to replace a 2,048 byte screen character buffer in 1/10 of a second we now expect a 1024 x 768 (or larger) display with 256 (or more) colors be updated in the same time frame. If we are to believe the hype of multi-media, this will get even worse when the performance standard is raised to real-time, true color (24 bits per pixel) color display. This explosion in use of graphical user interface (witness Windows 3.x growth) is unlikely to change.

Third, the relative density and cost of dynamic memory has outpaced the other major storage devices in desk-top systems; the magnetic disk by a factor of two or three-to-one. What is interesting about this last trend is the lack of improvement in raw performance of dynamic memory compared to its many-fold improvement in density.

What do these factors mean to us as users of the chip sets? We have to make decisions about the construction of the machine we are building based on the trends and outlook. For desktop systems, and particularly the bus structure of the system, this has led to a re-partitioning of the computer and a hierarchy of busses. Each of these busses has a different purpose and characteristic. Processor local busses are optimized for performance in latency and throughput but lack the capability of expansion. The ISA bus shines in its ability to support devices from a wide range of manufacturers. It still is limited in its expansion capability (about eight slots), and the user interface for installation and configuration is still rooted in the 1970s of jumpers and configuration switches. Systems have also been developed with internal busses for the specific purpose of communicating with dynamic RAM.

Not only have these diverse busses come into existence in a PC architecture, but the relationship between them has become more complex. In many ways, system design considerations are made by the designers of the silicon that makes up the core logic chip. Fortunately (or not) most of the successful chip set developers make sure

that they spend time with their major customers who often have a better perspective of the end user's needs, the manufacturing issues, and the hardware and architectural issues affecting their systems. This feedback allows the chip set companies to begin addressing such issues as the graphical user interface and high speed memory interface to dynamic RAMs. Many of the integrated system controllers being offered today allow for some degree of isolation between the system bus (ISA or EISA), the dynamic memory bus, and the processor bus. Intel's second-generation EISA bus chip set added the capability for multiple-way interleaved dynamic memory as well as read and write buffers in the data path parts that attach to both the processor and the EISA buses.

Isolating buses is a standard computer architecture technique for increasing system performance; many of the techniques in use today were applied to the designs of mini-computers of the seventies. As computer architecture evolved, the use of a memory-direct bus was one of the first features added to the systems.

Many of the participants in the early meetings of PC/ET later became involved in the consortium to develop the EISA definition. EISA retained the concept of extending the AT bus and sharing signals with the original bus. At the same time, definition was made for the ISA (Industry Standard Architecture) covering the IBM PC/AT sixteen bit bus. EISA is positioned as a response to IBM's Microchannel architecture, and attempts to add definitions and mechanisms to address features supported by the Microchannel and other system busses. These features include geographic or reprogrammable addressability, a configuration memory and I/O space for each card, and standard ways of including adapter-specific code in the operating system. Besides performance (33 MByte /Sec ), one of the goals of EISA is to allow sufficient configuration register space and configuration files to permit controllers to be installed without setting any jumpers or switches.

### ***DRAM Price Trends***

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The dynamic memory business is dominated by a commodity sales environment. For that reason, the successful manufacturers have highly-automated foundries that focus on a specific type of production run. The volume of the standard DRAM packages have driven the type of memory available in personal computer systems. These standard configurations of DRAM support access to the device either one bit at a time or four bits at a time. This configuration limitation restricts the minimum memory increment that can be added to a system using either discrete devices or Single Inline Module (SIM) multi-chip boards. For a thirty-two bit processor (386 DX or 486 SX/DX) system, the minimum memory increment for four megabit technology is four megabytes (presuming 1 Meg x 4 DRAMs).

Specialized DRAMs for video applications (VRAMs) support a mode of operation in which a selection of 256 bits can be stored in a shift register and shifted out of the RAM at video speeds.

One immediate alternative for achieving higher bandwidth from the dynamic RAM is to select dynamic RAMs that are configured as four bit wide devices. Therefore, for the same size of memory, a design can have a single bank of "by one" memory or four banks of "by four" memory and the ability to interleave them. Interleaving memory means that when a reference to a block of data is made, all the memory devices are accessed; the first comes from the first group and the second from the next. This form of memory configuration requires that different memory devices hold the data for memory locations that are one word apart. The benefit is that for a two or four word access, the time to complete all the transfers is cut in half or a quarter. This benefit has attached to it the two-fold penalty of additional power consumption and the restriction on the minimum amount of memory, or minimum increment, in a system.

Newer memory (DRAM) controller chip sets support many combinations of different sizes of memory in different banks. Many of these controllers will automatically attempt to optimize the "layout" of the memory and its relationship to the system address so that the highest performance can be accomplished.

Another configuration of DRAM that is beginning to emerge in the industry is the byte and sixteen bit wide devices. These parts will allow a finer granularity to the increment of memory that is added to a system. With 32 bit CPUs and memories being the standard, and 16 MBit technology around the corner, wider versions of DRAMs will be needed to support a system that is quite adequate with a total of four megabytes of system memory (1 MByte x 32 bits).



DRAM Prices	16 KBit	64 KBit	256 KBit	1 MBit	4 MBit
1978	11.0				
1979	7.5				
1980	6.0	37.0			
1981	5.8	21.0			
1982	1.9	9.0			
1983		6.0	55.0		
1984		2.1	31.0		
1985		1.7	10.0		
1986			9.8	64.0	
1987			9.5	37.0	
1988			9.0	26.0	
1989				14.0	45.0
1990				9.0	23.9
1991				4.7	18.3

*Price Per Megabyte, Technology Shown*

***Table 1.4: DRAM Prices, Cost Per Part***

Year	16K Bit	64K Bit	256K Bit	1 MBit	4 MBit	Cross- Over	\$/ MByte	% Decrease Ave: 73%
1978	5,632						5,632	
1979	3,840						3,840	68%
1980	3,072	4,736					3,072	80%
1981	2,944	2,688				<--	2,688	87%
1982	972	1,152					972	36%
1983		768	1,760				768	78%
1984		268	992				268	35%
1985		217	320				217	81%
1986			312	512		<--	312	
1987			304	296		<--	296	94%
1988			288	208			208	70%
1989				112	90		90	43%
1990				72	47		47	53%
1991				37	36	<--	36	76%
1992							18.3	50%
1993							9.2	50%
1994							4.6	50%
1995							2.3	50%
1996							1.2	50%
1997							.6	50%
1998							.3	50%

***Table 1.5: DRAM Prices, Cost Per Megabyte***

Not only has the onset of Windows and graphical user interfaces (GUI) driven up the demand for video performance, the need for additional system memory has been fueled by the increasing complexity of software and the ability of newer operating environments to support multiple tasks concurrently running on the system. Fortunately for the user, the cost of dynamic memory has continued an extreme downward trend starting in the early eighties.

## *Chapter 2: Chip Set Selection Criteria*

This book focuses on the silicon solutions that are available on the market for designs that are a superset of the IBM PC/AT which utilize 80286, 80386 and 80486 processors.

The application of each design drives the decision criteria for a chip set and the whole system design. Some of these criteria are straight-forward and are often forced by the application. First, we will review the obvious criteria, such as board real estate, power, performance, and cost.

One of the more difficult areas to assess relates to the make or buy decision. The factors involved not only include the cost of development, but also the need of product developers to differentiate their product from others in the field. Embedded personal computers, where the computer is a part of a larger product, often do not have the requirement that the computer portion of the product be distinctly different, except that unusual interfaces may be supported.

How does one differentiate a system architecture? There are many approaches to making a product unique; some are based on how the system is sold (offering better service, lower prices, or a better warranty often sells systems in today's market). Discussion of product differentiation as it relates to marketing, sales, and support is left to the reader. The issue of service does enter into the picture, however. How reliable the system is and how easy it is to correct any field failures of the system can have a profound effect on the viability of a design.

This issue of ease of service also relates to the issue of modularity. Recently, several personal computer manufacturers have identified the added benefit of modularity in the design of their personal computers.

Certain aspects of the personal computer architecture have not significantly changed from the original six megahertz PC/AT computer. Even the most powerful 50 MHz '486 machines that are based on the ISA bus require certain logic that is common to this original design. The 8259 interrupt controller, two 8237 DMA controllers, and the extension logic are all present in these systems.

The following table shows the elements found on the original IBM PC/AT Model 339 (8 MHz AT). These elements have continued to be present in personal computer compatibles ever since then. To this basic system, users added video, floppy disk, serial port, parallel port, modems, printer ports, hard disk, and additional system memory.

Part Number	Manufacturer	Description
I-82284	Intel	Clock Generator and Ready Logic
I-80286	Intel	Central Processing Unit
I-80287	Intel	Floating Point Co-processor (Optional)
I-82288	Intel	Bus Driver and Control Logic
I-8237A-5	Intel	DMA Controller (Qty 2)
74LS612	T.I. and Others	Register File (DMA Address Map)
I-8259A	Intel	Interrupt Controller
I-8254-2	Intel	Timer
I-8042	Intel	Keyboard
MC-146818	Motorola	Real Time Clock and RAM
DRAM		DRAM System Ram Chips
74F280		Parity Generator/Checkers (DRAM)
EPROM		32K x 8 Sockets 16 bit wide
74ALS245		Data Byte Lane Buffer
74ALS245		Address Buffers
74ALS573		Address Buffer/Latches
74LS646		Data Buffers 286 to Data Bus
74F257		Address 20 Mask (Note 1)
82S147N		Memory Control PAL
74ALS245		Memory Data Buffers

*Note 1: A20 Mask (also called A20 Gate)*

*Masking the Address Bit Twenty allows the system to simulate the operating environment of the 8088 (and 80286) in the "real" operating mode. The active low A20 mask output forces the host to mask physical address bit 20. A20 Mask is sourced by a bit of a control port or the keyboard controller.*

***Table 2.1: PC/AT Components List***

## *Chapter 3: Off the Shelf versus ASIC Approach*

When considering the design approach, the designer should be aware of the options that are being presented by the ASIC vendors. Traditional semiconductor companies were caught off-guard with the advent of companies such as LSI Logic, which offered a path for system developers and their designers to begin creating silicon solutions that incorporated and replaced many standard circuits.

With this initial success at the hands of the standard products vendors, ASIC (Application Specific Integrated Circuit) vendors rode a wave of significant growth and caused a shift in the way many computer companies develop PC-compatible personal computers.

The decision for developing ASICs is an expensive proposition. The cost of developing an integrated circuit not only includes the expense of non-recurring engineering (NRE) charges paid to the foundry company, but also the cost of in-house engineering resources which must spend six months or more creating a design and seeing it through the prototype and part qualification. The cost of this process easily can exceed \$100,000 per design.

Recent developments in field-programmable gate arrays have given designers an alternative to semi-custom development. A combination of standard parts plus field-programmable gate arrays allow designers to enter production much earlier than with traditional ASIC development. The approach does have its limitations, particularly in the area of semiconductor propagation delay. Typical worst-case commercial delays exceed five to seven nanoseconds per gate. On the other hand, currently-available gate arrays have a propagation delay of approximately 1.5 nsec per gate. With system performance becoming such a dominant selling point for systems, this additional gate delay may not be acceptable.

Another approach that often provides the best of both time to market and lower overall cost as well as system performance is the use of high speed programmable logic (such as PALs) combined with standard chip set components. After the product has proven itself in the marketplace, the programmable logic can be replaced with a semi-custom solution to decrease costs. This approach helps separate the overall product development risk from the ASIC development risk. Traditionally, semi-custom chip development has suffered from the phenomenon of meeting simulation specification at the time the design is "signed off" for fabrication, but not meeting some system requirement for the application. Statistically, this happens approximately fifty percent of the time. Prudent planning for an ASIC development would include one iteration of the design, which typically takes one week to debug, and another few days to incorporate in the design, simulate, and add test vectors. In the meantime, the balance of the design

would have to be proven to be correct. After this is done, there remains the process of "signing-off" the design with the ASIC vendor, laying out the physical design of the part, generating masks, and producing a new prototype. This iteration process easily adds six weeks to the point at which a design can be put into production.

On the positive side, the reward for having developed a unique and more cost-effective solution than the competition can be a considerable increase in market share. In the area of personal computer design, this is becoming increasingly difficult to do. The market is maturing, and the competition for developing winning chip sets is one in which companies are willing to invest millions of dollars. Many of these companies have gone even further and developed processors that emulate the '286, '386, and even '486 instruction set. These companies have invested tens of millions of dollars to pursue this market.

In summary, developing an ASIC will require an investment in the following areas :

- Design engineering: eight to thirty weeks (or more)
- Simulation and chip sign-off: six to twenty weeks
- Capital investment for chip prototype: \$15,000 (and up)
- Additional time to production from prototype delivery: twelve to sixteen weeks.

## Chapter 4: Processor Cache Circuits

Cache memories are designed to contain recently-requested data in a higher speed memory to improve the average access time for fetching instructions and data from main memory.

Terms used in this section are defined in the following paragraphs:

- Line Size:** This is the amount of data, usually expressed in bytes, that is moved into a cache memory. The principle of a processor cache memory is that references tend to be Temporal Local (local in time) or Spatial Local (local in space or address) to other references. Loading just the requested data into a cache addresses the issue of temporal locality since we are likely to reference the same data again soon. By picking a line size larger than the requested data we are likely to "pre-fetch" data that will be used shortly because of its spatial locality to the original data.
- Hit Rate:** The hit rate reflects the percentage of the references that are currently held in the cache memory versus those stored in some lower level memory (i.e., DRAM). The hit rate is usually expressed as a percentage, and for most implemented cache schemes exceeds 80 %. The miss rate is one minus the hit rate, so for a hit rate of 95% the miss rate is 5%.
- Miss Penalty:** When an access is made and the data is not available in the cache memory of interest, the time (either in nsec or clocks) taken to retrieve the data from main memory is called the miss penalty.
- Traffic Ratio:** The traffic ratio is a ratio of the amount of data moving between the processor and the cache versus the amount of data moving between the cache and the main system memory. The traffic ratio is expressed as a fraction: main memory transfers divided by the CPU-to-cache memory transfers.

Traffic ratio is a function of both the hit rate and the line size, and can be affected by the application that is running. For example, if the hit rate is high but the line size is excessively large, the amount of data being brought in from main memory (DRAM) can be larger than the amount of data that is being transferred to the processor.

When this is the case, it indicates that speculative retrieval of data is being made (to fill the cache line) but that the data is seldom referenced by the processor.

The traffic ratio is an often-ignored aspect of cache memory design but can have an important impact on system performance. Increasing the line size tends to increase the hit rate, but after a certain point, typically around 32 to 64 bytes depending on many factors, the traffic ratio begins to increase and the total memory bandwidth from main memory (DRAM) can begin to be the limiting factor.

**Write Policy:** Write policy refers to how write data is placed back into the main system memory. Two of the most common policies are Write Through and Write Back. In a "Write Through" policy, whenever the CPU performs a write operation on a data element (word), the cache controller or bus controller initiates a write operation to the main system memory. In the case of a "Write Back" cache memory, the modified data is held in the cache (only in the cache) until such time as that entry is replaced by a different data element. At that time, the cache line is tested (based on a status flag for each line) to see if it has been modified since it was brought into the cache. If it has, the data is "written back" to the main system memory.

Write back cache memories have become much more prevalent in the PC marketplace due to its additional performance gain over write through policy. This performance improvement comes largely from the case where a write operation is followed immediately by a second write operation.

In early implementations of the write through cache, the processor was stopped while the write operation was completed to the main memory (taking about 250 nsec or more). Later implementations of the write through cache memory used a scheme called buffered writes. With a Write Through / Buffered Write policy, the first write that affects a data line in the cache updates the cache copy and is also stored in a "write buffer". At this point the processor is allowed to continue processing and the cache controller manages writing this data to the main system memory.

If a subsequent write operation occurs before the first operation is complete, the next operation is "stalled" until the previous write operation takes place.



Write policy also has an effect on cache coherency. In a system where only one element in the system (the CPU) writes to system memory, cache coherency is not an issue. However, as PCs become more sophisticated, and the use of controllers (such as mass storage controllers) that are intelligent and write to system memory become more widely used, this issue must be addressed. Most PC cache implementations either cause all "Master Mode" DMA operations to use the cache (thus maintaining coherency), or cause any write access to a memory line that is contained in the cache to "invalidate" that cache line entry. This invalidation causes the CPU to re-fetch the data from the main memory if it needs the data again.

**Associativity:** The associativity of a cache memory system refers to the way data is replaced and the restrictions on the way data is stored in the cache. In an ideal case, the cache memory would be fully associative, and only the "n" most recent access from the CPU would be stored in the cache. In this case, there would have to be a comparator for each of the lines of data in the cache memory. In practice, this is not a cost-effective use of the silicon. Typical applications of cache circuits use a mechanism that limits the number of compare operations that have to take place to determine a cache hit. The following Associativity models exist:

**Direct Mapped Cache:** For any given address generated by the CPU, there exists only one entry in the cache that can be used for the caching of that data. This is done to simplify the compare logic to determine a cache "hit". The implementation of this type of cache uses a fixed field of the CPU address to select a tag entry and the balance of the CPU address to be compared against the tag entry contents. This approach has the disadvantage in the case where two data structures are being operated on that would "map" into the same cache line and cause the cache controller to constantly swap between the two data values in that cache.

**"N" Way, Set Associative:** An "N" way (such as two way) set associative cache refers to a cache that divides the cache memory into "N" separate blocks of cache each with a separate tag comparator. This scheme allows multiple data elements that would map to the same cache line entry in a Direct Mapped Cache to exist in the cache at the same time. The greater the number, the more associative the cache is, and the greater the support logic requirement to maintain and update the cache.

Fully Associative: In fully associative caches, as described above, the cache line is capable of holding any data value from anywhere in the system memory. This approach is rarely used due to the extreme cost of the control logic and the small gain over "set associative" approaches.

In the personal computer market, the trend for higher-end systems has been to develop '486 machines with a second-level external cache that implements a write back policy as described above. Additionally, trends in the semiconductor industry and the pricing of larger, very fast static RAMs have driven the PC cache architecture toward a common solution. Most PC implementations use either direct map or two way set associative cache memories. The implementing of a two way set associative cache has several penalties associated with it. First, there needs to be twice as many cache data and tag compare RAMs in the system. Typical pricing of static RAMs (SRAM) has decreased for larger size RAMs such that the system implementer can afford to put a single SRAM that is four or sixteen times larger than the two of the smaller SRAMs required for a two way associative cache memory.

One of the "rules of thumb" mentioned in the excellent book on computer architecture by David A. Patterson and John L. Hennesy (*Computer Architecture: a Quantitative Approach*) is the "2:1 Cache Rule" which states the following :

*The miss rate of a direct-mapped cache of size  $X$  is about the same as a 2-way-set-associative cache of size  $X/2$ .*

From this, we can see that the system architect of a high-end PC would be as well or better off to use a direct mapped cache of larger size, particularly if the direct cache was four times larger than the two way set associative cache.

Another effect that tends to bode in favor of using a direct mapped cache is the way the data is accessed in the cache. In both direct mapped caches and set-associative caches, the access of the data and the tag look-up / compare take place in parallel. With today's faster processors, the hardware generally makes an assumption that there is going to be a "hit" (a good assumption for 90+% hit rates) for reads and begins presenting the data to the processor. If it turns out the data is not in the cache, the cache memory is disabled from driving the processor bus and simultaneously the data is accessed from main memory. There is no performance penalty for the assumption of a hit. However, with a two way (or more) cache, until the tag look-up and compare is made, the cache controller does not "know" which cache SRAM to enable to the processor bus. This adds to the delay for accessing the cache memory and often means either an additional clock cycle for cache accesses or the use of faster (and more expensive) RAMs in the set-associative approach than the direct mapped approach to cache memory.

## *Cache Write Policy*

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A cache write policy refers to conditions under which a particular cache line is moved (or copied) back to the main system memory. Three of the most common cache write policies are Write Through, Write Back, and Posted Write.

A write through cache system returns data that is modified in the processor cache to the system memory. This means that read operations can take advantage of the cache memory but write operations still have to wait on the latency of the system memory. The difference between a cache memory access and a main memory access (for the write through) is often a factor of five to one. The cache can often respond in 30 nsec (33 MHz) where the main system memory responds in 150 to 200 nsec. With the advance state of the art of integrated external cache controllers available from multiple sources, today's standard in the industry is to supply an external write back cache on 486 systems.

Intel's '486 uses an internal write back cache scheme. For this reason, most system vendors have chosen to augment this internal write through cache with an external cache memory that is both larger and features write back capability.

A write back cache works in a different way with respect to updates to the main system memory. When a data element (line of the cache) is placed in the cache, even when it is modified, the data value is not written to the main system memory until that entry in the cache is required by a system reference that needs to be placed in that cache entry. So instead of immediately placing the modified data back in the system memory, the operation is deferred until that cache entry is no longer needed. The nature of computer programs is that they tend to operate on data "local" to other data that they have operated on. Because of this phenomenon (Locality of References), a write back cache line may accumulate multiple modified data values before being "flushed" back to the main memory. This write back policy has better performance than the write through performance. Part of the cost of this higher performance is the additional complexity of keeping track of when an entry in the cache has been modified and under what conditions, when devices like bus master controllers modify the contents of the cache line.

## *Cache Associativity*

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Cache associativity refers to the degree of freedom that the cache control logic has on placing data in the cache. In the case of a direct-mapped cache, certain address lines are used for a "selection" of the particular cache line. If two data elements that

were commonly being processed by a CPU have the same address in the range used to select the cache line, they could not coexist in the cache memory.

### *Cache Coherency*

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By introducing a second copy of data stored in the system (within the cache) there is also introduced the possibility of having these two copies of the data becoming "out of sync", or differing in content. In the system environment, DMA or bus mastering devices can modify the main memory (DRAM) copy of the data while the copy that is held in the processor or cache memory is not modified. This problem is solved in several different ways by the personal computer chip vendors. The simplest is to have the DMA or bus master "invalidate" any copy of the data that exists within the processor (for '486) or cache memory. This is the approach taken by the Intel 82385 Cache controller. Another method for dealing with this problem is to cause all references to main memory, whether from the processor or from bus mastering devices, to use the cache. This approach has the benefit of improving the performance of both DMA and processor accesses as well as maintaining cache coherency.

Multi-processing systems that have cache memory local to the processors but use a shared memory must use a more comprehensive mechanism for support of cache coherency. Two basic approaches that are used are Centralized (directory based ) and Distributed (MESI or MOESI protocol). The directory approach requires that the system main memory include a control mechanism and directory that keeps track of the ownership of each block (cache line) of the system memory. If an access of a memory block is detected to be either shared or owned exclusively by another element in the system, the centralized controller generates a request to cause the current owner of the data to return the data to the main system memory.

In the Distributed approach, each element in the system keeps a status of the data held in the local cache(s). Multiple copies of a data element can exist within the system. However, before any element can modify a given element of data, it must first become the exclusive owner of that data element. This process is where the terms MESI and MOESI are derived. They are acronyms for the different states that the cacheable memory element can take on while being held in a cache memory:

**M:** *Modified* - owned exclusively and has been modified

Eventually, this copy will be either flushed back to the main system memory or will be transferred to another element for exclusive ownership and modification.

**O:** *Owned* - owned not yet been modified, no other outstanding copies have been made.

*E: Exclusive* - owned exclusively for the purposes of modification

*S: Shared* - this copy of the data element is one of more than one that exist in the system (beside the main system memory) and it may not be modified before acquiring exclusive ownership.

*I: Invalid* - this copy of data is invalid.

Most commonly this happens when another element has acquired the data exclusively and all other copies must be marked invalid so that only the copy owned exclusively can be modified.



## *Chapter 5: Quality*

The issue of quality of a semiconductor product is one of the most difficult to measure but among the most important to track. Consider the effect on the company, and your job, if, after selecting a vendor for an integrated personal computer solution and shipping tens of thousands of products, it turns out that the vendor supplying your PC chip set does not have control of process, quality, or supply.

Most of the suppliers listed in this guide have quality programs and a separate department responsible for assuring the quality levels of the products being shipped. This issue is so important that most companies assign the group responsible for quality a high level (Vice President or Director) leader. Doing this insures a level of autonomy from other groups within the organization.

There are several areas that a prospective customer can inquire about to determine a vendor's commitment to providing a quality product. Some vendors may be unwilling to share certain aspects of the data due to the potential compromise of proprietary data. This is an extremely competitive business and most vendors will take extra precautions before disclosing or making available certain data about their product or procedures. In the case of test vectors, for example, it is unlikely that a customer would be able to get a copy of the test vectors used on the part unless that customer were an acknowledged, large volume consumer who does not fabricate their own chips and is willing to receive the vectors under a non-disclosure agreement.

### *Test Vectors*

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Test vectors are the stimuli that are applied to the integrated circuit after it is fabricated and before it is packaged. The test vector set includes the expected response from the chip when these input stimuli are applied. As you can see, the test vector set is a road map and a detailed description of each function within the chip.

Test vectors fall into several types. The two main types of test vectors are functional, which exercise each and every function within the chip but are typically not run at the full rated speed of the part. Another type of test vectors is the "high speed" vector set. These vectors are only run against the packaged, completed part. Some vendors combine the functional and high speed vectors, which generally gives a better level of protection for failures. However, this approach often does not significantly increase reliability or quality, but adds to the cost and time for developing the test vectors.

## ***Fault Coverage***

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Fault coverage is a measure of the degree to which the test vectors will detect errors or flaws in the silicon. The method for determining fault coverage is to first simulate the part using all of the test vectors used for production testing. This pass of results is saved as the "golden" copy (no faults). A fault simulation is then run, where internal nodes of the design are systematically artificially "faulted" and the simulation is run again. The fault simulator then determines if the given fault would have been detected by the test vectors that are used in production of the part. This process can be very time-consuming and compute-extensive. Fault simulation was once only done on aerospace and military designs due to the extreme amount of computing costs.

Many different techniques have been developed to speed up the process. Fault simulator art has been advanced to the point where faults that are not dependent on each other can be simultaneously simulated, simulations are run only as far as the first miss-compare, and statistical methods make fault simulations much more practical. Additionally, the extreme increase in computing power since the early eighties has brought fault simulation to the commercial market.

Statistical fault simulations that have been run against as few as five per cent of the nodes in a design have been shown to be a sound method of analysis. Designs that have been carefully designed and carefully simulated typically only yield a fault coverage level of eighty to eighty-five percent. To bring the fault coverage to industry standard levels of ninety-five percent takes a special effort. Finding out what fault level coverage a design has is a good indicator about commitment to quality.

## ***AQL Levels and Quality Plan***

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Another measure of a vendor's commitment to providing a reliable source of product is their Quality Plan and their AQL levels. Vendors should be willing to discuss their plan and the methods they use to assure delivery of quality product. This can be a very educational process, as most vendors have staffs of professional, well-qualified quality assurance team members.

## **Compatibility Verification**

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Related to the issue of quality is the issue of compatibility of the design with existing personal computers. Several companies specialize in the business of



compatibility testing. Many larger companies involved in the development of compatible personal computers establish their own internal compatibility testing labs. Compatibility must be measured for both software operation and expansion bus compatibility.

Software compatibility is often determined by verifying the operation of the target system running operating system software as well as certain applications. The following list is typical of software run to verify the compatibility of a computer.

D-BASE III	Rel 1.1
Lotus 123	Rel.2.0
IBM PC/AT Advanced Diagnostics	
Auto Cad	Rel 10
Turbo C	Rel 1.0
OS/2	Ver. 1.1
SCO UNIX 386	System V
MS-DOS	Ver. 3.0
MS-DOS	Ver. 3.3
MS-DOS	Ver 4.1
MS-DOS	Ver 5.0
Novell Netware 386	Ver 3.11
Microsoft Flight Simulator	
Windows	Ver. 2.2
Windows	Ver. 3.0, 3.1 and Windows NT

***Table 7.1: Compatibility Test Software***

Hardware compatibility for add-in cards is more difficult to verify. Basic timing can be verified, however, assuring that the final design meets the interface specification over the entire range of temperature, voltage, and process variation. CMOS semi-conductors will vary from 50% to 180% of typical delay. This represents more than a three-to-one variation of the delays in the chip. Verification often relies on using circuit simulation. The simulator can be controlled to set the delays to either the fastest or slowest possible delay (under all conditions).



## ***Chapter 6: Personal Computer versus Workstation Architecture***

With the onset of more sophisticated operating systems for the personal computer, the market for workstations and personal computers is on a collision course. The workstation manufacturers are now looking for a target market to expand beyond the scientific and engineering marketplace. The PC marketplace represents a market more than ten times that of the workstation market in volume. For that reason, price pressure is considerably higher for the personal computer market.

One of the interesting aspects of the workstation marketplace and Sun SPARC Stations specifically, is the phenomena of the system developer having complete control over the partitioning of the system and the levels of integration and performance required for each element. In some ways, this architecture represents the direction personal computer architecture will take as the goals of higher levels of integration and lower cost are pursued.

Recently-announced trends in the PC bus architecture will enable the PC platform to come closer to the workstation in the levels of integration. Traditionally, the processor design has been "owned" by Intel and there was very little coordination of the architecture between Intel and core logic chip set companies. The proliferation of alternate sources for the '386 and '486 architecture and pressure to reach higher levels of integration have changed the nature of the business. Intel's recent announcement of the PCI (Peripheral Component Interface) standard will allow PC compatible machines to be built with less overhead of interfaces and a higher level of integration.

With PCI, standard peripherals can be integrated into a system main board using a pinout that only requires forty-nine pins for a full-performance, in excess of one hundred megabyte, peripheral bus. This shift in the architecture of the personal computer creates an opportunity for the silicon vendors to continue the push toward a system where the mainstream computer is developed with just a handful of components and system memory. The next few years will see a distillation of the designs toward that trend. This newer architecture will begin to make the difference between the personal computer and the workstation less distinct.

Traditionally, the following characteristics have separated workstations from personal computers in their focus:

### Workstation Requirements :

- 1) Large Main Memory Capacity
- 2) Floating Point Performance

- 3) Large Screen / High Resolution Display
- 4) Large amount of Mass Storage
- 5) Optimized for UNIX
- 6) Open / Semi-open graphical user interfaces
- 7) Networking

In contrast, the business computer applications have placed a premium on a different set of criteria. These more often focus on cost and productivity. The decision as to what type of computer is used in the business application often has more to do with training time and ability to run graphical applications (such as business graphics). This is one of the reasons that Apple has enjoyed the success it has in the business management arena. High quality business presentation and document preparation software has been available on the MAC long before it was available on the PC platform.

Business Computer Requirements:

- 1) Commodity Product (low cost)
- 2) Controllability of the System Resources
- 3) High Quality Presentation / Documentation Packages
- 4) Ease of user training and support

Engineering / Science Requirements

- High performance integer processing
- High performance floating-point processing
- Large physical memory capability
- Graphics presentation capability
- Networking
- Interface for non-standard instrumentation

### *Cost Performance of Personal Computer versus RISC*

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Ultimately, the reduced instruction set (RISC) versus complex instruction set (CISC) argument will be based on performance and cost for that performance. Early proponents of the RISC architecture argued that only with RISC could certain CPU architecture features, such as concurrent execution of instructions, be achieved. As it turns out, there is no limitation of applying most of these CPU architectural features to a complex instruction set. The difference is the number of transistors (and complexity) that is required. As the cost of silicon becomes lower and lower, the difference in cost/performance of a RISC-based solution and a CISC-based solution will blur. Second order effects such as manufacturing capacity and quality, economies of scale (market size), and competition will have a greater effect on the cost of such systems.

Current-generation processors are routinely planned and executed with over a million transistors, and the next generation will treble that number. The additional overhead represented by a complex instruction set will become a smaller percentage of the silicon cost, and will continue the trend toward convergence of PC and RISC workstation architectures.

### *Windows Impact*

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As the presence of graphical applications and environments have made their way to the PC, the need for some of the workstation attributes have migrated to the PC. Main memory capacity, high resolution displays, and large amount of mass storage have all become considerations for newer PC platforms.

Graphical performance has especially become a focus of the industry with the tremendous gain in popularity of Windows. The performance levels expected by users has changed dramatically. At the same time, the idea of using loadable device drivers or hardware that is not bit-for-bit compatible with some existing standard has gained more acceptance. VGA solutions today typically include device drivers to take full advantage of their solutions.

The increased performance of video throughput is often addressed with hardware specific solutions for activity that slows down work on a graphical interface. Among these, the most common forms of acceleration are:

- 1) Higher bandwidth access to video memory
- 2) Intelligent video controller with support for graphics primitives such as bit blitter and fill.

Higher bandwidth access to video memory has helped to spawn the ISA-VL bus interface standard. Initially, this standard was developed primarily for direct access for the CPU to the video memory at the highest possible data rate. The second approach is universally applicable for both slower system busses and high speed local busses. A large gain can be realized even on the ISA bus with a graphical accelerator. Placing that accelerator on the local bus also adds the benefit of the high bandwidth local bus interface.

The combined trend of acceptability of drivers usage and the use of Windows type of user interfaces increases the ability of hardware designers to make better software / hardware tradeoffs.

## *System Disk Performance*

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The PC systems of today have begun to take on the attributes of workstations in the area of disk size and performance. The original PC/AT used a five megabit per second, three-to-one interleave disk to provide data. The data transfer rate from this drive was less than 200 KBytes/second during the data transfer phase of a disk access. Newer disks have improved that number to forty megabits per second and now have a transfer rate that can exceed four megabytes per second. When the improvements in seek time (40 msec to 12.5 msec average) and rotational latency (8.6 msec to 6.3 msec) are taken into account, the disk performance improvement has not kept up with the tremendous increase in processing performance.

With the growing acceptance of drivers and non-strict adherence to the register level compatibility, users have begun to benefit from faster drivers and software-based disk caching that accelerate the apparent access rate of the disk. With these changes have come the increasing acceptance of the SCSI interface in the personal computer. Again, this trend causes the distinction to blur between the RISC workstation and the personal computer. For the foreseeable future, most PCs will still use the Integrated Drive Electronics (IDE) interface to attach to the disk. This trend is bolstered with the advent of thirty-two bit drivers and disk cache software that comes bundled with Windows 3.1.

Integrated Drive Electronics interface has also recently received a boost from the EISA working group and certain disk drive manufacturers when a definition of a "Type F" data transfer was created specifically for the IDE drives. Instead of taking five or six clock cycles (at 8.333 MHz) to transfer a sixteen bit file, the "Type F" allows a word to be transferred every three clocks for an effective transfer rate of just over five megabytes per second. Typical performance for the disk transfer without this type of transfer is about two megabytes per second. As the disks have become faster, this has become a bottleneck in the performance of a disk. This change in the specification allows system designers to substitute a new version of the I/O chip in the system design and take advantage of the greater transfer rate performance.

## *Chapter 7: Level of Integration and Cost*

Chapter Three, "Off the Shelf versus ASIC Approach", describes some of the considerations that a system builder must evaluate to determine the level of engineering effort to be placed on the system development. Weighing the other end of the spectrum is the effect of alternate sources for a given solution and the resulting price pressure. If a vendor of integrated circuits is able to offer a product that no other vendor has, and that product has a clear price or performance (or both) advantage over the alternatives, that vendor can charge a premium for that solution. However, when the same pin-for-pin and functionally-equivalent part is available from a several manufacturers, the vendor is forced to sell the product based on different criteria. These criteria include quality, delivery schedules, terms, and, of course, price.

That price differentiation leads us to the discussion of the offerings in the chip set arena. One of the early solutions for the core logic of the original PC/AT was a chip pioneered by Chips and Technologies. This part is known as the 82C206, and includes the functional equivalents of the Intel 8237 DMA controllers (2), the DMA mapping register, the Intel interrupt controller, and counter / timer circuit. These elements, together with some standard decoding and support functions, were combined in the '206. Several manufacturers, including Intel, have added to this basic function with such features as the real time clock / battery backed-up RAM that was originally provided by the Motorola MC-146818 stand-alone part. In addition to several enhanced versions such as the Intel part, the original 82C206 has been copied in function and pin interface by several other manufacturers. Considerable price pressure has now forced the price in quantity to nine dollars or less. Considering the functions included in this part, it is a very reasonable price. Few other parts in the PC chip set category, with the exception of dynamic memory SIMs, have become such commodity items.





## *Chapter 8: Low Power Considerations*

There are several tactics to achieve low power consumption. With the widespread use of CMOS logic, most of these strategies center on either turning off inactive circuitry or reducing the clock frequency of that circuitry to reduce switching current consumption.

In the seventies, many computer systems were designed with TTL and Bipolar logic families. These logic families were well-known for the speed performance they delivered, but had the distinct disadvantage of consuming a tremendous amount of power.

Advancements in semiconductor processing technology and lithography have allowed the CMOS process to catch up to the faster but more power-hungry technologies. With CMOS, the logic elements are built out of MOS field effect transistors (FETs) which have very little leakage current between the gate and drain when they are switched on. Due to this characteristic, CMOS power consumption is directly tied to the frequency at which it is switching.

New power-saving circuits from various chip set manufacturers have gone to great lengths to reduce the switching frequency in power-sensitive applications. One tactic is to have the system monitor its own activity and processing demand. If the demand is light, the system can run at a slower clock frequency. For this reason, earlier laptop systems allowed the user to set the speed at which the processor was running.

Intel introduced a version of the 386 processor called the 80386SL that supports power management via a "System Management" mode. This architecture focuses on power savings with disk, display, and components that are not part of the CPU.

## *Power Management Issues*

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Many chip sets being marketed today offer features to help conserve power consumption. The various levels of operation and power consumption are typically defined by the following levels. Each level in the table below describes the power conservation level, the actions taken at that level, and the activity that will put the computer in that level of power conservation.

1. **Power Off**: Power switch shut-off.
2. **Full Power** Mode.
  - Enter / Keep state: keyboard activity
  - Exit to **Slow**: Low CPU demand
3. **Slow**: Slow system clocks. (Typical sequence: 20 MHz -> 10 MHz -> 5 MHz)
  - Enter: Low CPU demand
  - Exit to **Standby**: No-keystrokes timer expired
4. **Shutdown**: Shut down peripheral circuitry.
  - Enter: No peripheral activity (either keyboard or I/O)
  - Exit to **Full Power**: keystroke activity
  - Exit to **Standby**: No-keystroke-activity timer
5. **Standby**: Turn off display
  - Enter: No peripheral activity (either keyboard or I/O)
  - Exit to **Full Power**: keystroke activity
  - Exit to **Sleep**: No-keystroke-activity timer # 2 and no peripheral activity
6. **Sleep**: Save register and RAM data to disk
  - Enter: No-keystroke-activity timer # 2 and no peripheral activity
  - Exit to **Resume**: resume switch
7. **Resume**: Restore register and RAM data from disk
  - Enter to **Resume**: resume switch
  - Exit: on completion of restore to **Full Power**

Activity Monitors typically monitor I/O decodes to determine computer activity.

1. LPT1:	378 hex to 37f hex
2. COM1	3F8 hex to 3FF hex
3. COM2	2F8 hex to 2FF hex
4. Keyboard Reads	060 hex (reads)
5. Floppy I/O	3F0 hex to 3F7 hex
6. Hard Disk I/O	1F0 hex to 1F7 hex

***Table 8.1: Typical Power Down Monitor Ports***

Power control integrated circuits are designed to allow the processor to detect when a particular part of the computer is inactive and turn the power off to that part of the computer to help conserve battery usage. The mechanism uses power output control pins that are designed to be connected to the gate of a power FET (Field Effect Transistor).



## Chapter 9: Performance

Recently, the most common measure of personal computer performance has become the measure of millions of instructions per second (MIPS). Not too long ago, the use of MIPS was only found in the domain of the mainframe. When personal computers were introduced, their computing power was generally considered to be in the area of four hundred thousand instructions per second (0.4 MIPS).

The following two tables give the reader a feel for the relative computing performance of today's processors relative to the mini-computers of the seventies and eighties. Various benchmarks have been established for the measurement of computing power. Suites of tests such as the AIM performance benchmark and the Neilson Nelson suite of system benchmarks present a more accurate picture of actual performance in a system environment. Each of these benchmarks are tuned to a particular type of computing task. Both the AIM and Neilson Nelson have components of the test for I/O, scientific type, and business type computing. Another standard which is becoming well-known is the SPEC (System Performance Evaluation Cooperative). This industry standard benchmark is also a combination of ten separate benchmarks, and the final value assigned to a machine is a geometric mean of the suite of benchmarks, normalized to one (for a VAX 11-780).

Computer	Year	Linpack	Drystone
AT/386-33	1991	0.48	15750
VAX 8550	1987	0.69	
VAX 8600	1985	1.43	
NCR PC486-33/MC	1991	1.50	35250
SPARC SLC	1991	2.25	18255
VAX-11/780	1978	4.90	
DEC Station 5000	1990	6.45	36670
IBM Power Station 320	1991	8.15	45454

*Table 9.1: PC and Minicomputer Performance*

System	Processor	Clock	MIPs
(generic)	486-DX2	33/66	26.7
EverexStepCube	486	33	21.7
CompaqDeskpro	486	33	20.0
CompaqDeskpro	486	25	16.0
ASTPremium	486	25	15.0
CacheComputers	486	33	14.6
EverexStep	486	25	11.1
EverexStep	386	33	8.3
CacheComputers	386	33	7.5
EverexStep	386	25	6.1
CacheComputers	386	25	5.7
ATTronics	386	25	5.7
EverexStep	386	20	4.9
EverexStep	286	20	4.2
EverexStep	386	16	3.2
EverexStep	286	16	3.2
EverexStep	286	12	2.5
(generic)	486	33	20.8
(generic)	486	25	16.2
(generic)	386	33	10.4
(generic)	386	25	8.1
(generic)	386SL	25	5.3
(generic)	386SX	20	4.6
(generic)	386SX	16	3.5

***Table 9.2: Intel Processor Performance***

John Hennessy and David A. Patterson, in their previously-referenced book on computer architecture, describe two different benchmark approaches to storage system performance. One type of benchmark, which is primarily applied to super-computers, measures performance using eight megabyte sequential file operations.

Another benchmark focuses on transaction processing. This I/O benchmark measures the performance of a computer system performing random 100 byte record accesses interspersed with sequential operations. For each transaction, the benchmark presumes from two to ten disk I/O operations and each disk operation takes between 5,000 and 20,000 CPU instructions. With a computer that executes fifteen million instructions per second, in order to keep up with the instruction-based transaction rate of over a thousand transactions per second, the disk subsystem would need to provide an I/O rate of three thousand I/Os per second.

To contrast that level of performance with the real world of current disk technology gives the reader an appreciation of the perceived need for disk storage subsystems and specialized cache support for the disk.

### *PC Benchmarks*

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Over the years since the original PC was introduced, several companies have brought to the market, either to sell hardware or as a stand-alone product, benchmarks that measure the performance of a system. Some of these are listed below:

Power Meter (Version 1.5)

Landmark (Version 1.14 )

PC Magazine (Version 5.5)

Norton SI (Version 4.5)

Byte Magazine (Version 1.3)

### *Intel Processor Relative Performance*

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Recently, Intel Corporation has developed a benchmark called the iCOMP. This is a single-index performance benchmark that combines with various weightings several of the other industry standard benchmarks (such as Ziff Davis / PC Magazine's). This benchmark includes 5% weighting for 32 bit floating point, 25% for 32 bit integer, 3% for 16 bit floating point and 67% for 16 bit integer operations. The index is designed to enable potential customers to quickly determine the relative computing power of a system based on the Intel processor family.

Intel Processor	Clock	iCOMP Rating
80486 DX2	66 MHz	297
80486 DX	50 MHz	249
80486 DX2	50 MHz	231
80486 DX	33 MHz	166
80486 SX	33 MHz	136
80486 DX	25 MHz	122
80486 SX	25 MHz	100
80486 SX	20 MHz	78
80386 DX	33 MHz	68
80386 DX	25 MHz	49
80386 SX	25 MHz	39
80386 SX	20 MHz	32

***Table 9.3: Intel Microprocessor Relative Performance***



## *Chapter 10: Chip Set Data Sheets*

This section contains systemized extractions from the data sheets for a large number of integrated devices. The data has been taken directly from information supplied from the manufacturer, and re-formatted to help you compare the functions available in the various devices. Information was received from the following vendors:

ACC Microelectronics Corporation  
2500 Augustine Drive  
Santa Clara, Ca 95054  
Phone : 408-980-0622  
Fax : 408-980-0626

Acer Laboratories, Inc.  
Phone: 408-432-6200  
FAX: 408-749-8032

Appian Technology, Inc.  
(was ZyMOS)  
Phone: 408-730-8800

Austec Microsystems  
2903 Bunker Hill Lane, Suite 201  
Santa Clara, CA 95054  
Phone: 408-988-8556  
FAX: 408-988-0818

Bull Micral of America Inc.  
900 Long Lake Road  
New Brighton, MN 55112  
Phone : 612-633-5660  
FAX: 612-633-6387

Chips and Technologies  
3050 Zanker Road  
San Jose, California 95134  
Phone : 408-434-0600  
Sales : 408-437-3300

Cyrix Corporation  
Phone: 214-234-8387  
800-848-2979

Edsun Laboratories, Inc.  
564 Main St.  
Waltham, MA 02154  
Phone: 617-647-9300

Elite Microelectronics Inc.  
4003 North First St.  
San Jose, Ca 95134-1599  
Phone : 408-943-0500  
Fax : 408-943-0561

ER & DC  
Electronics Research and Development Centre  
(A Scientific Society of Department of Electronics, Government of India)  
Vallayabalam Thiruvanthapuram 695-033 India  
Phone : 0471-60116  
0471-64810  
Fax : 0471-68569  
Intl Fax : 91-471-68569

ERSO  
Electronics Research and Service Organization  
Division of Industrial Technology Research Institute  
8th Fl  
315 Song Chiang Rd  
10477 Taipei, Taiwan, ROC  
Phone : 02-502-8212  
Fax : 02-502-8795

ERSO (In California )  
2950 Scott Blvd.  
Santa Clara, Ca 95054-3312  
Phone : 408-727-1280  
Fax : 408-727-1338

G2 / Headland Incorporated  
46221 Landing Parkway  
Fremont, CA 94538  
Phone : 408-433-8000

Intel Corporation  
3065 Bowers Avenue  
Santa Clara , Ca 95051  
Phone: 408-765-8080  
800-548-4725

MetaDesign Semiconductor  
2895 Northwestern Parkway  
Santa Clara, CA 95051  
Phone: 408-986-9000  
FAX: 408-748-1038

Micro Integration Corporation  
1015-C East Brokaw Road  
San Jose, Ca 95131-2310  
Phone : 408-453-7333  
Fax : 408-453-7339

Mosel  
914 West Maude Avenue  
Sunnyvale, Ca 94086  
Phone : 408-733-4556  
Fax : 408-733-2271

Motorola Incorporated  
Semiconductor Products Division  
3501 Ed Bluestein Boulevard  
Austin, Texas 78721  
Phone : 512-928-6888  
Fax : 512-928-7991

National Semiconductor  
2900 Semiconductor Drive  
P.O. Box 58090  
Santa Clara, CA 95052-8090  
Phone : 408-721-5000  
Fax : 408-739-6204

OPTi Incorporated  
2525 Walsh Ave  
Santa Clara, CA 95051  
Phone : 408-980-8178  
Fax : 408-980-8860

PLX Technology Inc.  
625 Clyde Avenue  
Mountain View, CA 94043  
Phone : 1-800-759-3753  
Phone : 415-960-0448  
Fax : 415-960-0479

Siemens Components Incorporated  
2191 Laurelwood Road  
Santa Clara, CA 95054  
Phone : 408-980-4500  
Fax : 408-980-4596

Suntac  
Sun Electronics Corporation  
250 Asahi Kochino-Cho  
Konan-City Aichi, 483 Japan  
Phone : (0587) 55 - 3331  
Fax : (0587) 55 - 3851

Symphony Laboratories  
2620 Augustine Drive Suite 250  
Santa Clara, CA 95054  
Phone : 408-986-1701  
Fax : 408-986-1771

Texas Instruments  
PC Systems Logic  
8339 LBJ Freeway  
P.O. Box 655303, MS 8328  
Dallas, Texas 75265  
Phone : 214-997-5086

UMC  
United Microelectronics Corporation  
No. 3 Industrial East Third Road  
Science-Based Industrial Park  
Hsinchu City, Taiwan, R.O.C.  
Sales Phone : 02-715-2455  
Fax : 02-716-6291

UMC  
US Branch : Unicorn Microelectronics Corporation  
3350 Scott Blvd.  
Buildings 48 & 49  
Santa Clara, CA 95054  
Phone : 408-727-9589, 408-727-9239  
Fax : 408-492-1720, 408-970-0548

Vadem  
1885 Lundy Avenue Suite 201  
San Jose, CA 95131  
Phone : 408-943-9301  
Fax : 408-943-9735

VLSI Technology Inc.  
1109 Mc Kay Drive  
San Jose, CA 95131  
Phone : 408-434-3100



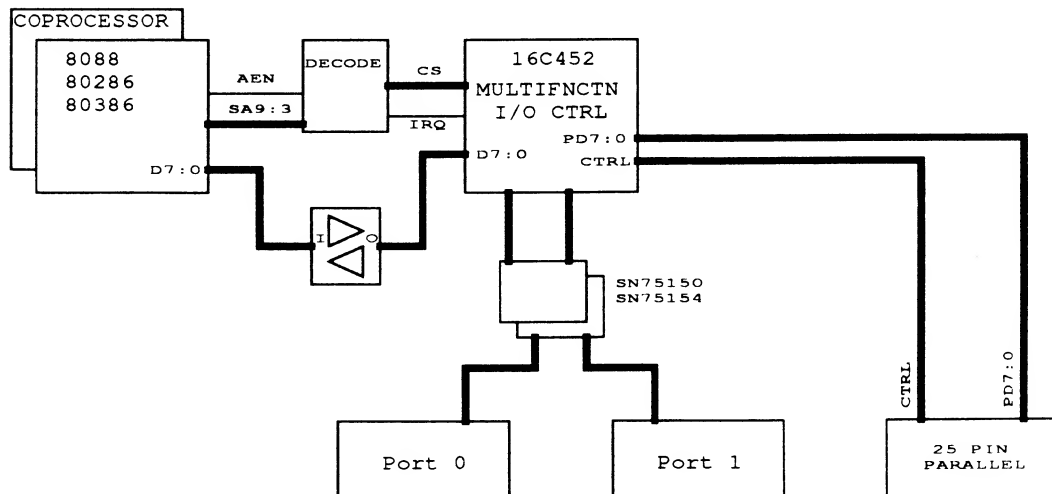
**Manufacturer:** ACC Microelectronics  
**Processor Supported:** 8088, 80286 & 80386SX  
**System Bus:** AT  
**Part:** ACC 16C452, Multifunction I/O Control Chip for PC.XT.AT  
**Availability:** 1988

**Cache:** No  
**Clock Speed:**  
**Main Memory Support:** No

**Second Source:** 100% compatible with NS 16450 & NS 8250.

**Functions Contained:**

Supports PC/XT/AT port address decoding	Programmable serial interface characters
(2) Serial ports	(1) Parallel port
(1) full-duplex asynchronous receiver/transmitter	Supports Double buffering in character mode
Centronics printer interface	Parallel port extended mode with bidirectional I/O
Parallel port supports readable input pending status	Direct drive for parallel port interface



ACC 16C452 Multifunction I/O Control Chip

**Manufacturer:** ACC Microelectronics

**Processor Supported:** 8088, 80286, & 80386

**System Bus:** PC/XT/AT and PS/2

**Part:** ACC 16C451, Multifunction I/O Control Chip

**Availability:** 1988

**Second Source:** 100% compatible with NS 16450 & NS 8250.

**Functions Contained:**

Supports PC/XT/AT port address decoding

(1) Serial ports

Independent control signals for each port

Supports Double buffering in character mode

False start bit detection

Centronics printer interface

Parallel port supports readable input pending status

**Cache:** No

**Clock Speed:**

**Main Memory Support:** No

Programmable serial interface characters

(1) Parallel port

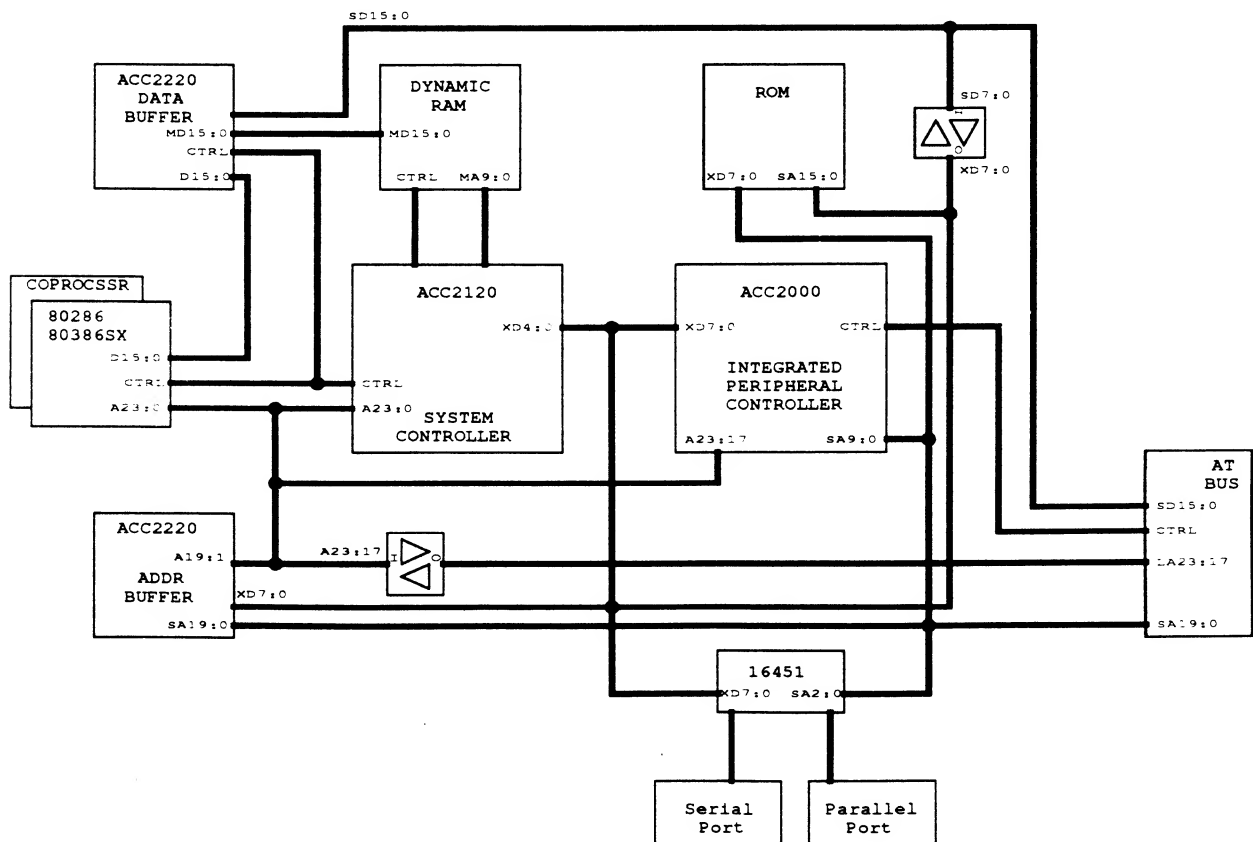
(1) full-duplex asynchronous receiver/transmitter

Full modem control support

Programmable baud rate

Parallel port extended mode with bidirectional I/O

Direct drive for parallel port interface



ACC 82020 Chipset



**Manufacturer:** ACC Microelectronics

**Processor Supported:** 8088, 80286 & 80386SX

**System Bus:** AT

**Part:** ACC 16C461, Multifunction I/O Control Chip for PC.XT.AT

**Availability:** 1989

**Second Source:** 100% compatible with NS 16450 & NS 8250.

**Functions Contained:**

Supports PC/XT/AT port address decoding

(1) full-duplex asynchronous receiver/transmitter

Programmable baud rate

Double buffering in character mode

Centronics printer interface

Parallel port supports readable input pending status

Programmable serial interface characters

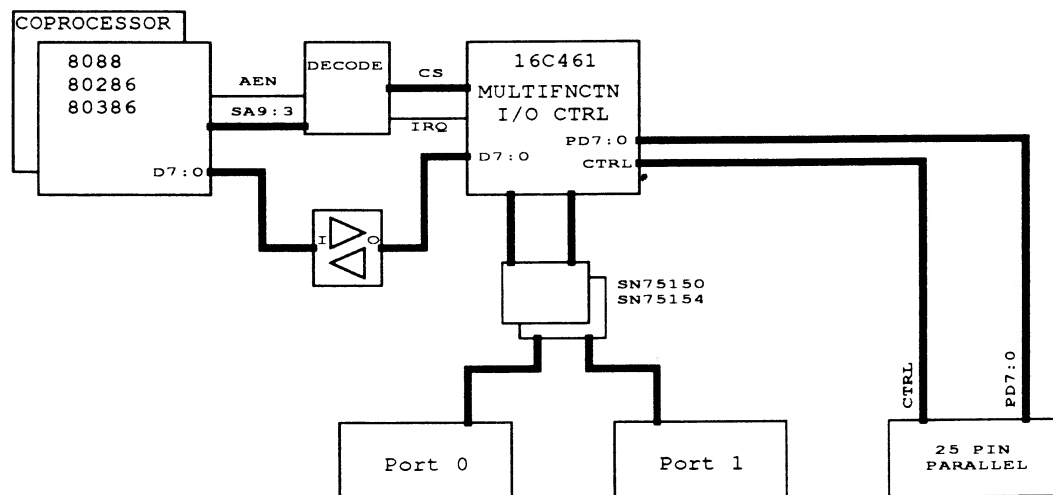
Supports single crystal clock input

Full modem control functions

False start bit detection

Parallel port extended mode with bidirectional I/O

Direct drive for parallel port interface



ACC 16C461 Multifunction I/O Control Chip

**Manufacturer:** ACC Microelectronics

**Processor Supported:** 80286, 80386SX

**System Bus:** AT

**Part:** ACC 2000, PC/AT Integrated Bus & Peripheral Controller (part of 82020 & 823000 chipsets)

**Availability:** 1988

**Second Source:**

**Functions Contained:**

100% compatible with IBM PC/AT

(2) 8237 compatible DMA controller

(2) 8259 compatible Interrupt Controller

Supports 8 MHz DMA clock

Built in refresh control

**Cache:** No

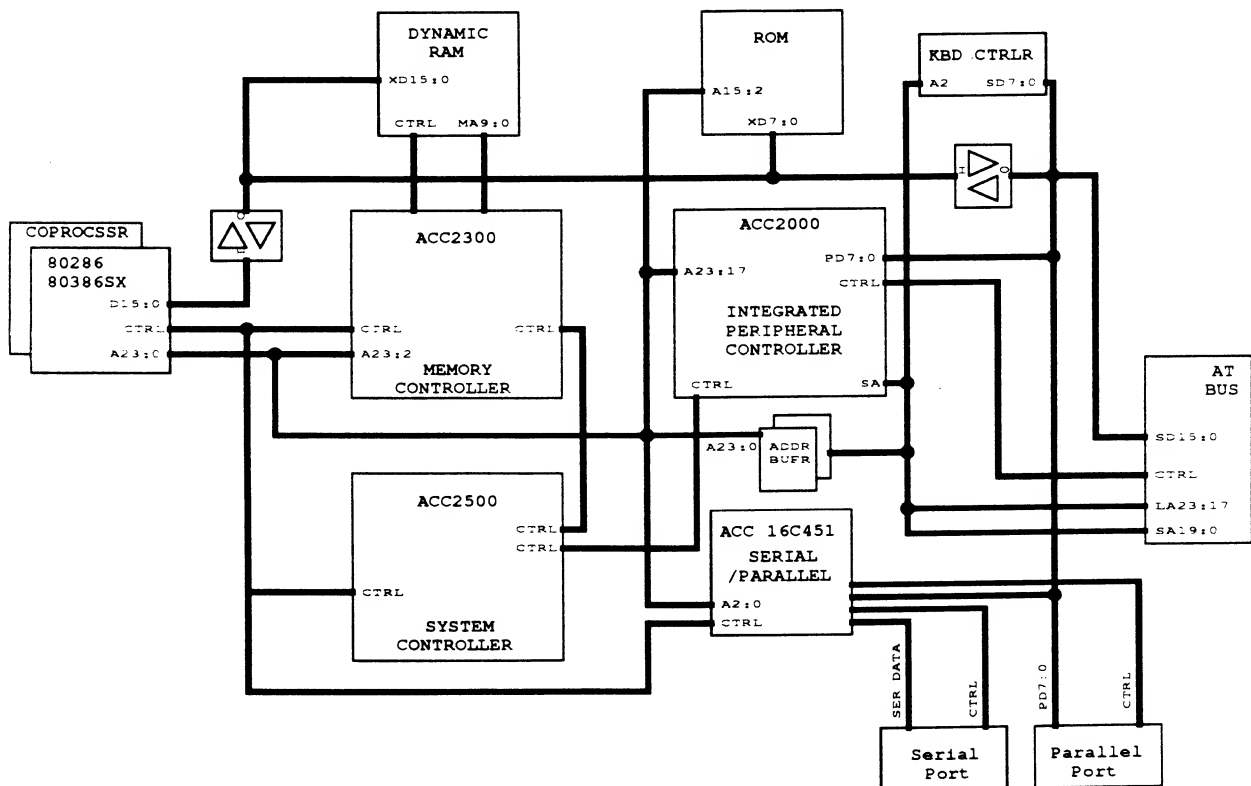
**Clock Speed:** 25 MHz

**Main Memory Support:** No

(1) 8254 compatible Timer/Counter

(1) 74LS612 compatible Memory Mapper

Supports up to 16MB DMA space



ACC 82300 Chipset

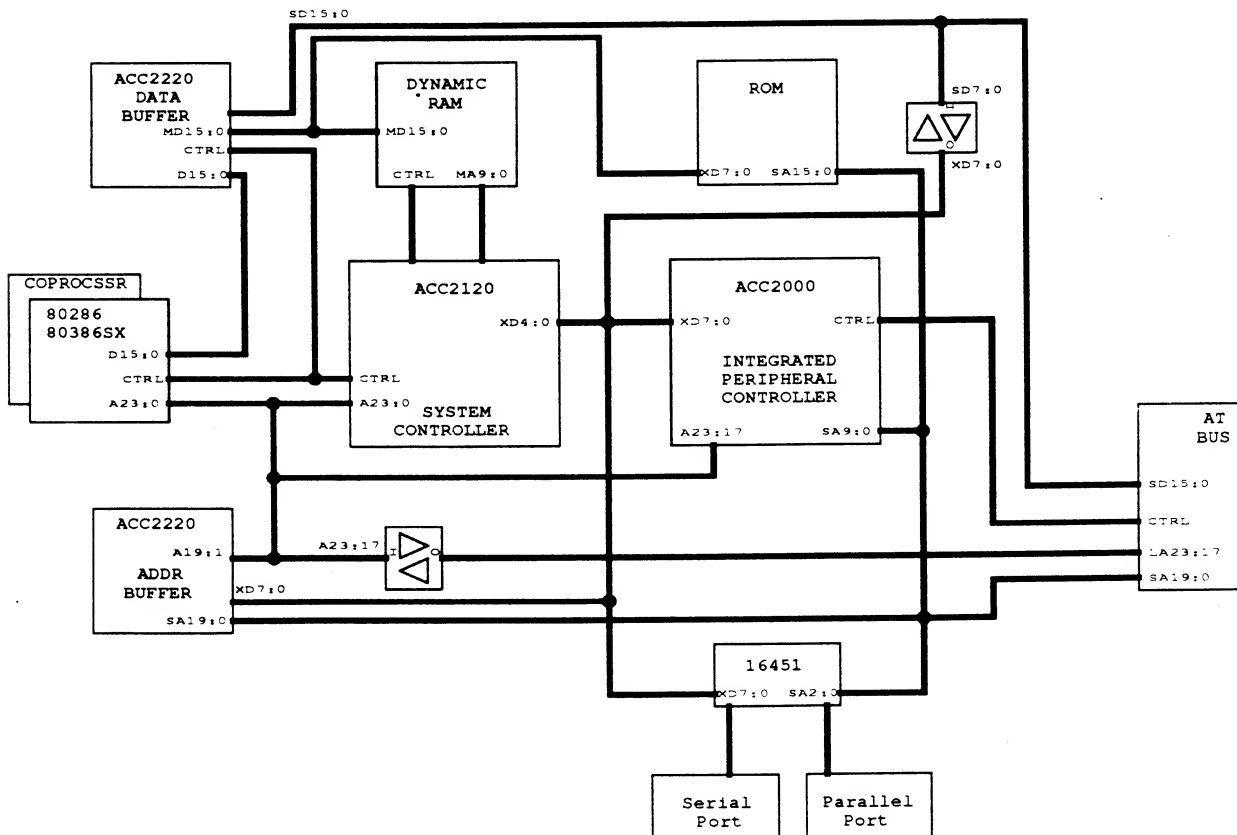
**Manufacturer:** ACC Microelectronics  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT  
**Part:** ACC 2120, PC/AT Integrated System Controller (part of 82020 chipset)  
**Availability:** 1988

**Cache:** No  
**Clock Speed:** 25 MHz  
**Main Memory Support:** Yes

**Second Source:** fully compatible with Intel's 82888bus controller

**Functions Contained:**

100% compatible with IBM PC/AT	Built in 80287 interface logic
Built in command delay & wait state generation	Supports upto 16 MB on board
Hardware/software turbo switch	Simultaneous extend and EMS memory support
Supports EMS 4.0	Staggered memory refresh
1-way, 2-way, 4-way page interleaved memory controller	Supports shadow RAM
Programmable wait states for ROM	ROM chip select
384KB Memory mapping above resident RAM	
Supports 64Kx1, 256Kx1, 256Kx4, 1Mx1, 1Mx4, 4Mx1 DRAMS	



ACC 82020 Chipset

**Manufacturer:** ACC Microelectronics

**Processor Supported:** 80286, 80386SX

**System Bus:** AT

**Part:** ACC 2220, PC/AT Integrated Data & Address Buffer (part of 82020 chipset)

**Availability:** 1988

**Second Source:**

**Functions Contained:**

100% compatible with IBM PC/AT

Data (3) buffers & (1) latch

Built-in parity generation/detecton logic

Hard disk, floppy, serial, parallel chip selects

**Cache:** No

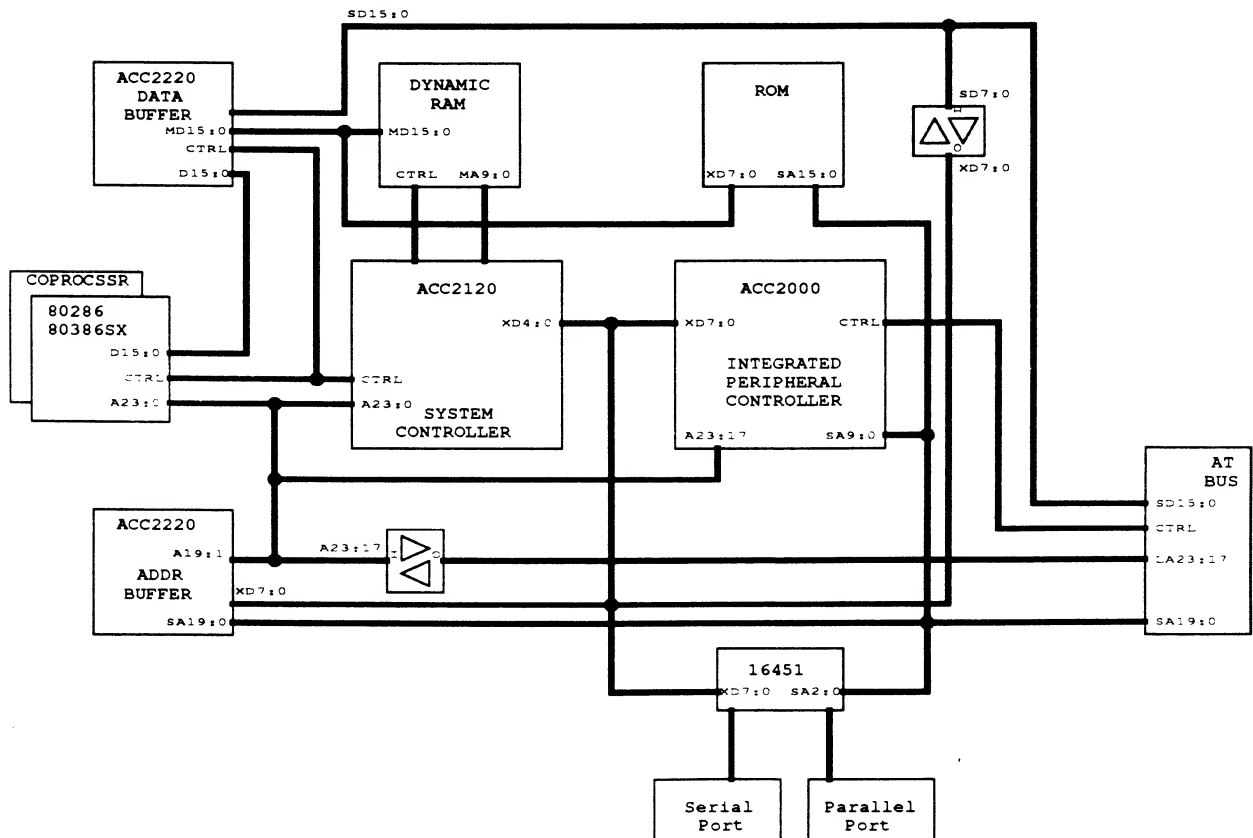
**Clock Speed:** 20 or 25 MHz

**Main Memory Support:** Yes

Address (1) buffer & (3) latches

Bus-conversion logic (16- to 8-bit transfers)

Supports high drive for expansion ports



ACC 82020 Chipset

**Manufacturer:** ACC Microelectronics

**Processor Supported:** 80386

**System Bus:** AT

**Part:** ACC 2500, System Controller

**Availability:** 1988

**Second Source:**

**Functions Contained:**

Independent 8 MHz AT Bus clock

CPU interface and Bus control

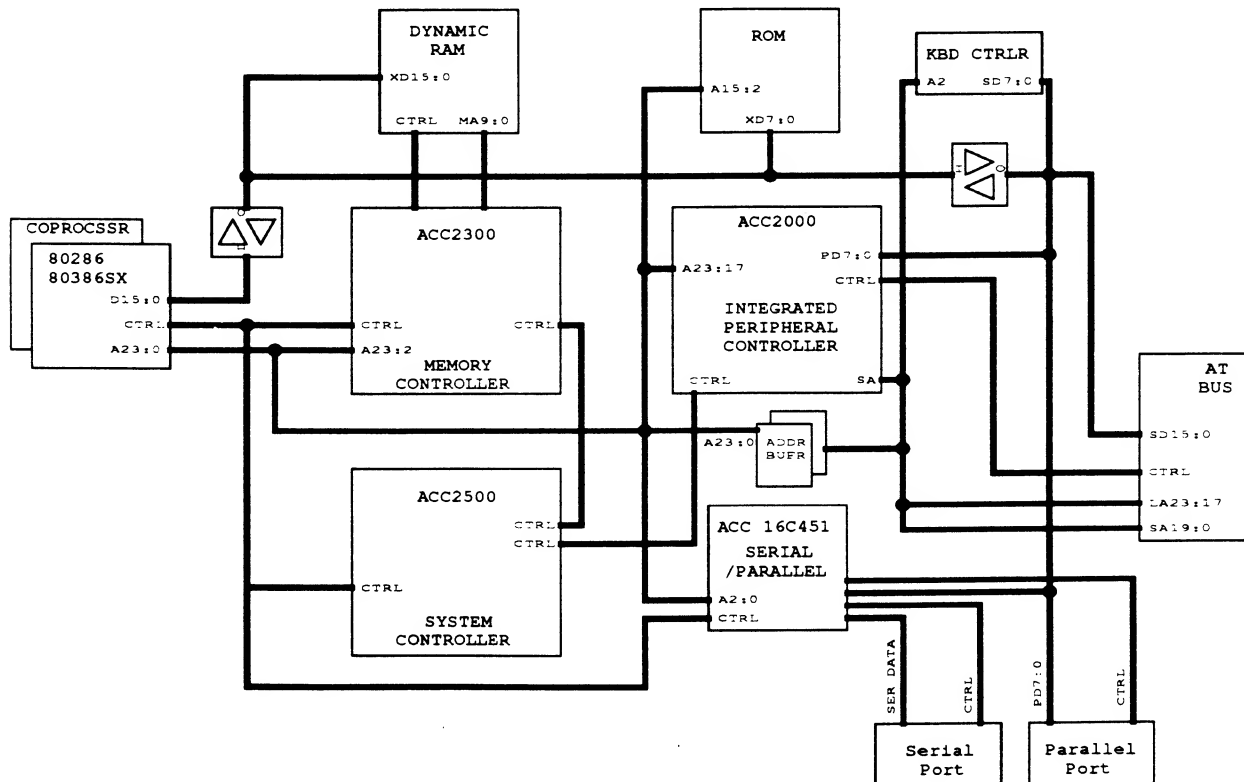
Reset and shutdown logic

**Cache:** No

**Clock Speed:** 20 or 25 MHz

**Main Memory Support:** No

20/25MHz or 8MHz processor clock selection  
AT Bus timing emulation



ACC 82300 Chipset

**Manufacturer:** ACC Microelectronics

**Processor Supported:** 80386

**System Bus:** XT/AT

**Part:** ACC 3201, XT/AT Floppy Disk Formatter/Controller

**Availability:** 1988

**Second Source:**

**Functions Contained:**

Supports 360K/720K/1.2M/1.4M formats

Supports up to (4) 3.5" or 5.25" floppy drives

Emulates NEC765A

Supports variable write precompensation

Contains on-dhip digital data separator

**Cache:** No

**Clock Speed:** 24 MHz (XTAL)

**Main Memory Support:** No

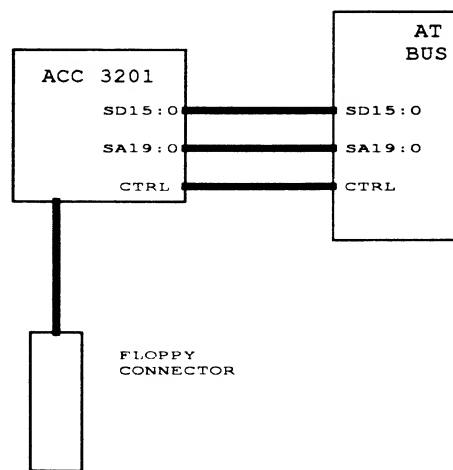
Supports data rates of 250, 300 and 500 K bits

Single 24MHz clock needed

Handshake support DMA (or non-DMA)

Built-in address mark detection

Programmable record length: 256, 512 or 1024 bytes/sector



ACC 3201 Floppy Controller

**Manufacturer:** ACC Microelectronics

**Processor Supported:** 8088/80286

**System Bus:** XT/AT

**Part:** ACC 1900, Turbo 80286 to 8088/8086 Processor Converter

**Availability:** 1988

**Second Source:**

**Functions Contained:**

Translates 16-bit data path into 8-bit path

Supports 80286 clock rates up to 16 MHz

DMA logic for 80286

Supports asynch operations (separate clock)

**Cache:** No

**Clock Speed:** 16 MHz

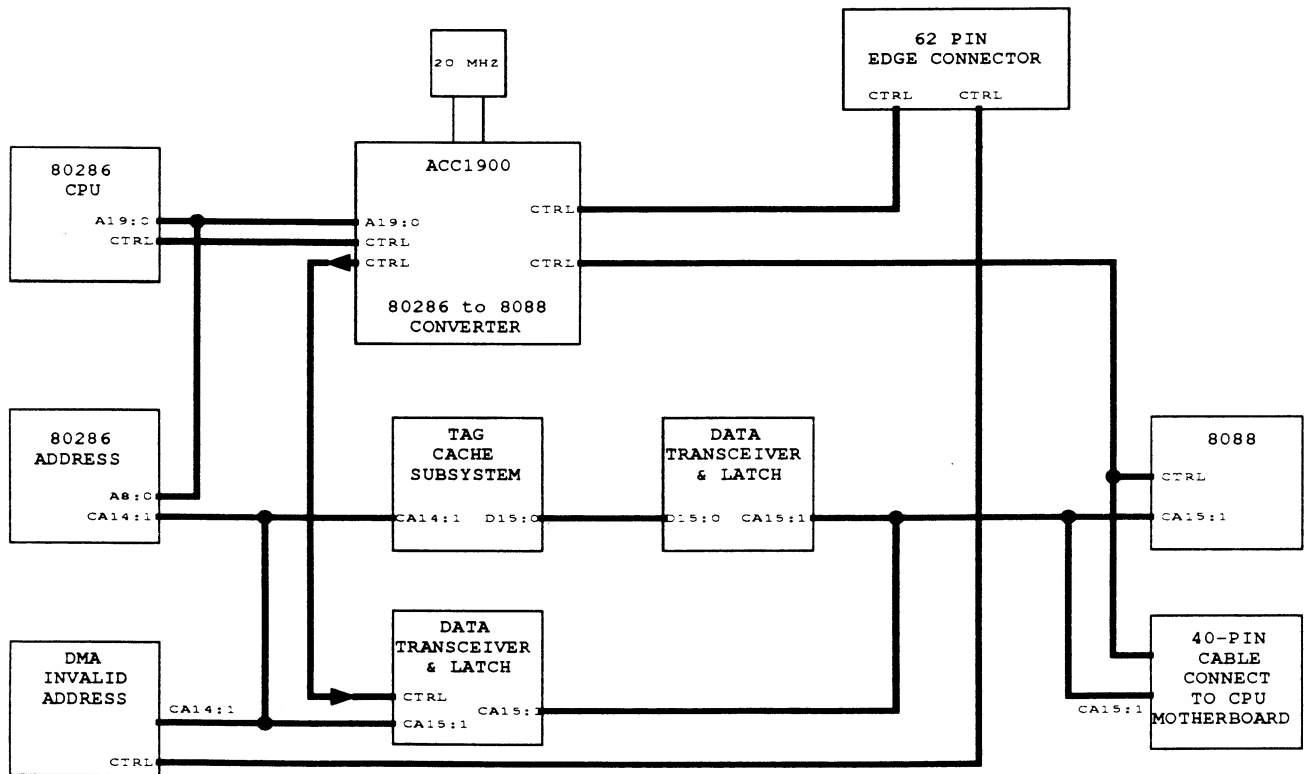
**Main Memory Support:** No

Cache logic supports 16KB cache

Supports 8088/8086 clock rates up to 10 MHz

Supports 80287

Hardware switchable between 8088 & 80286



ACC 1900 Turbo 80286 to 8088 Converter

**Manufacturer:** ACC Microelectronics

**Processor Supported:** 80386

**System Bus:** MCA

**Part:** ACC 5810, Micro Channel Interface Chip

**Availability:** 1988

**Second Source:**

**Functions Contained:**

100% compliance with IBM PS/2 implementation

Supports up to 256 I/O locations

Supports Burst DMA transfer

Supports 2 interrupt sharing sets (4 sources per set)

Supports POS Port Decode Logic & handshaking

Supports 4 programmable wait states

**Cache:** No

**Clock Speed:**

**Main Memory Support:** No

Supports up to 256 memory starting addresses

Supports 16 Arbitration requests

Implements level-sensitive interrupt sharing

I/O & memory mapping support

Supports channel check

Schematic Not Available At Press Time



**Manufacturer:** Acer Laboratories Inc.  
**Processor Supported:** 8088  
**System Bus:** XT  
**Part:** M1101, PC/XT Super Integration Chip  
**Availability:**

**Cache:** No  
**Clock Speed:** 8 MHz  
**Main Memory Support:** Yes

**Second Source:**

**Functions Contained:**

IBM PC/XT compatible  
Wait state and NMI control logic  
Supports 2764 and 27256 ROMs

Hardware/software CPU speed change  
Supports 64K, 256 K & 1M bit DRAMs  
Built in delay line for RAS, CAS and MUX

---

Schematic Not Available At Press Time

**Manufacturer:** Acer Laboratories Inc.

**Processor Supported:** 80286

**System Bus:** AT

**Part:** M1207-12/16, Super-Integration Single Chip For 80286-Based PC/AT System

**Availability:**

**Second Source:**

**Functions Contained:**

Page-interleaved (1 or 2-Way) memory support

0 wait state with 100ns DRAMs at 16 MHz

Configurable wait states & memory organization

Asynch or synchronous 8/10 MHz expansion bus clock

Fast A20GATE and RC support

16/8-bit BIOS ROM selectable switch

**Cache:** No

**Clock Speed:** 10-20 MHz

**Main Memory Support:** Yes

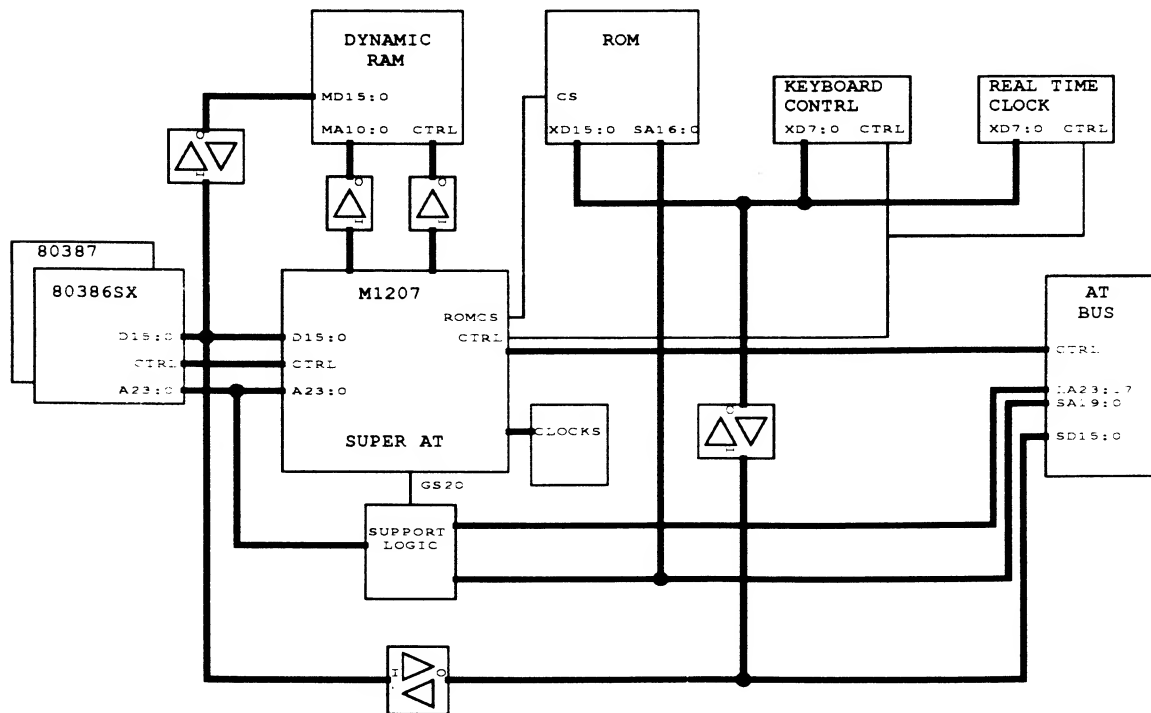
Supports 512KB to 8MB (64 K, 256K, or 1M bit)

0 wait state with 80ns DRAM at 12 MHz (no page)

Remapping/shadow RAM for BIOS

Supports staggered refresh

Supports LIM EMS 4.0



ACER m1207 Super Integration Single AT Chipset

**Manufacturer:** Acer Laboratories Inc.

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** M1209, 80386SX PC/AT Super-Integration Chip

**Availability:**

**Second Source:**

**Functions Contained:**

(2) 8237 compatible DMA controllers

(1) 8254 timer

16/20/25 MHz hardware/software speed select

Asynch or synchronous 8/10 MHz expansion bus clock

Remapping/shadow RAM for BIOS

Supports up to 8MB on board memory

Configurable wait states & memory organization

**Cache:** No

**Clock Speed:** 16, 20, or 25 MHz

**Main Memory Support:** Yes

(2) 8259 interrupt controllers

80387SX interface

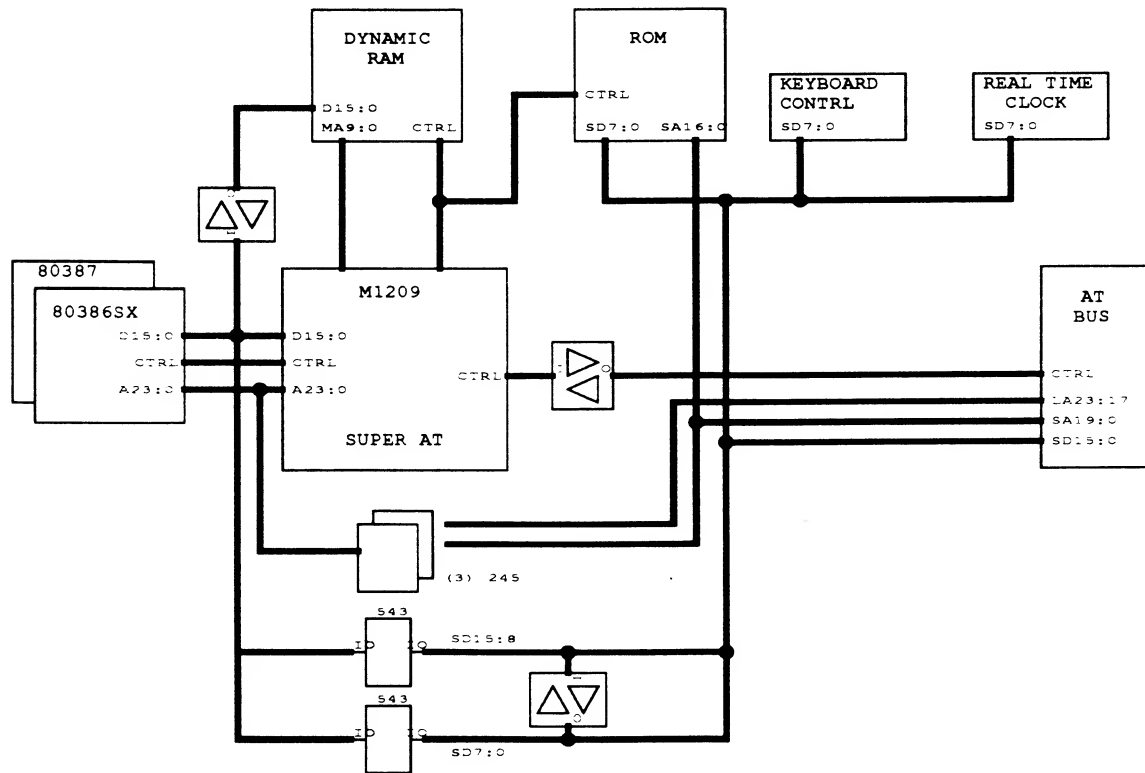
16/8-bit BIOS ROM selectable switch

Supports staggered refresh

Page interleaved DRAM controller

Parity generation/checking logic

Fast A20GATE and RC support



ACER 80386SX PC/AT Super-Integration Chip

**Manufacturer:** Acer Laboratories Inc.

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** M1385SX, 80386SX PC/AT Cache Controller

**Availability:**

**Second Source:**

**Functions Contained:**

Direct mapped (page size 16KB) or 2-way set associative (page size 8KB)

Snoop watching mechanism

Zero wait state read hit

Dual bus (frees CPU local during DMA)

Full 16MByte address mapping

**Cache:** Yes

**Clock Speed:**

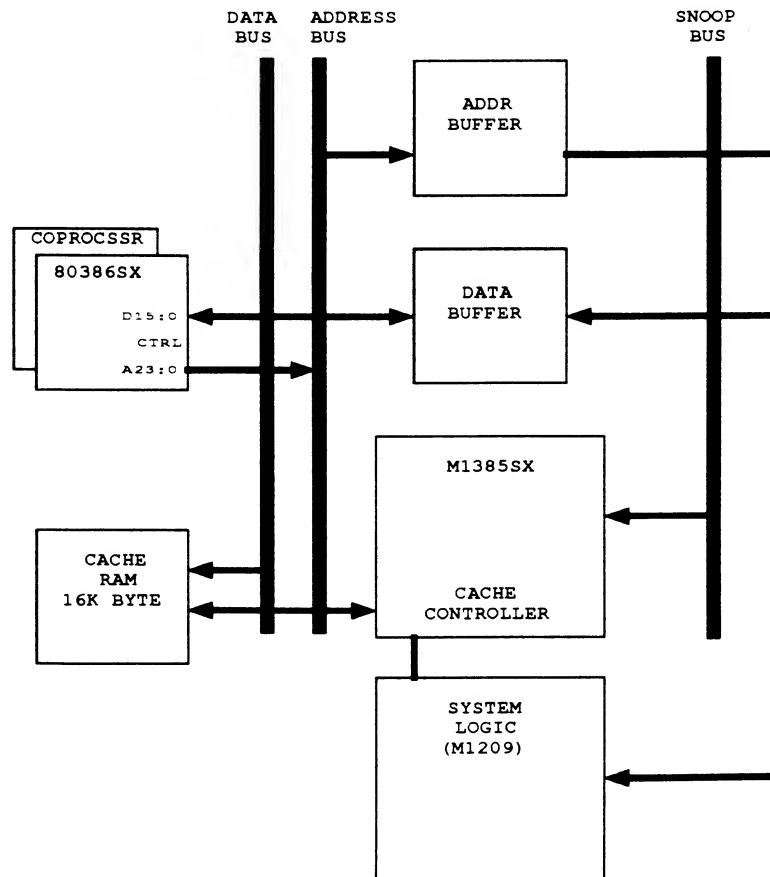
**Main Memory Support:** No

99% read hit rate

Zero wait state of posted memory write

Interface to non-cache system design

Non-cacheable memory support



M1385SX: 80386SX PC/AT Cache Controller

**Manufacturer:** Acer Laboratories Inc.

**Processor Supported:** 80386

**System Bus:** AT

**Part:** M1385DX, 80386 PC/AT 32K Cache Controller

**Availability:**

**Second Source:**

**Functions Contained:**

Direct mapped (page size 32KB) or 2-way set associative (page size 16KB)

Snoop watching mechanism

Zero wait state read hit

Dual bus (frees CPU local during DMA)

Mapping 32KB cache in onto 32MB main mem

**Cache:** Yes

**Clock Speed:**

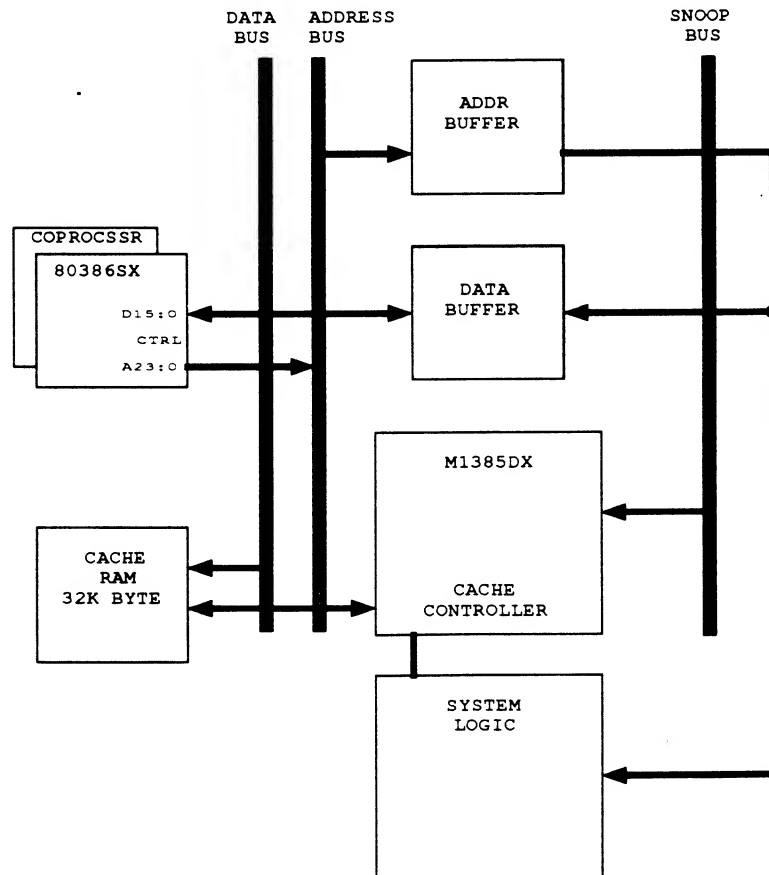
**Main Memory Support:** No

99% read hit rate

Zero wait state of posted memory write

Interface to non-cache system design

Non-cacheable memory support



M1385DX: 80386 PC/AT 32K Cache Controller

**Manufacturer:** Acer Laboratories Inc.

**Processor Supported:** 8088, 80286, 80386

**System Bus:** PC, XT, AT

**Part:** M5105, Super I/O

**Availability:** 1990

**Second Source:**

**Functions Contained:**

100% compatible with PC/XT/AT architectures

(2) NS16450 compatible UARTS (independent) Modem control functions

(1) Floppy Disk Controller (UPD765A & DP8473 compatible)

FDC supports 360K, 720K, 1.2M, & 1.4M byte formats On-chip data separator (1 Mb/s)

Bidirectional parallel port (for either printer or scanner)

Interface for embedded hard disk controller

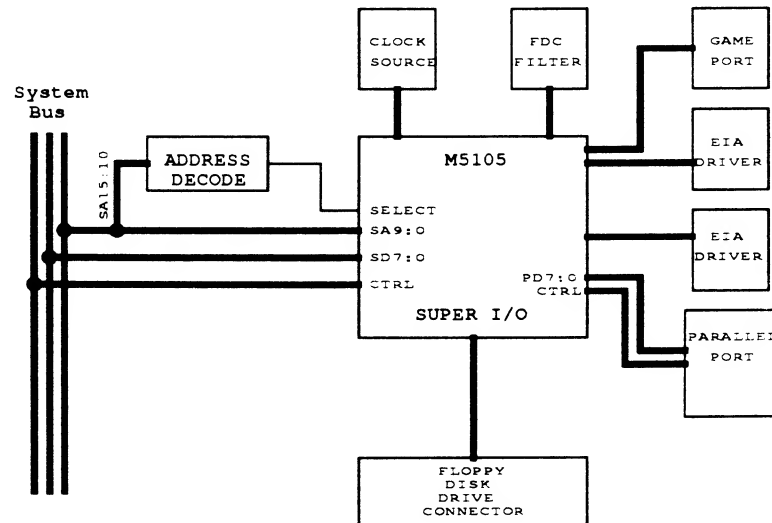
Game port decoding logic

DMA enable logic

**Cache:** No

**Clock Speed:** 24 MHz (XTAL)

**Main Memory Support:** No



ACER M5105 Super I/O

**Manufacturer:** Appian Technology

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** A90, Notebook Controller

**Availability:** 1990

**Second Source:**

**Functions Contained:**

On-chip peripheral AT coprocessor

Multiple (independent) device shutdown

Intelligent Look-ahead memory coprocessor

Supports memory from 512KB to 32 MB

**Cache:** No

**Clock Speed:** 16 & 20 MHz

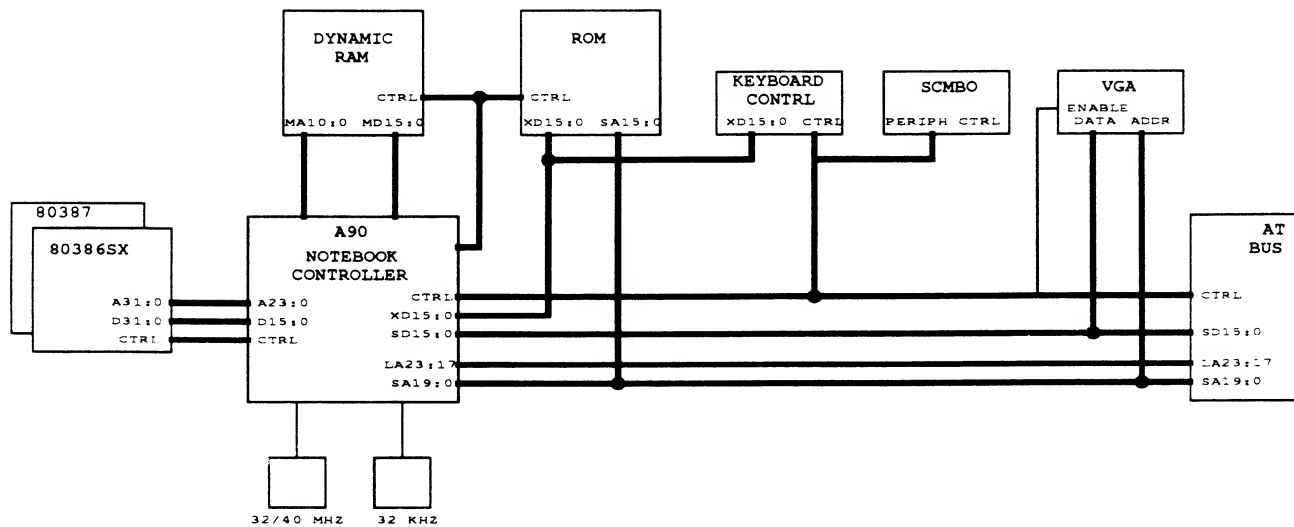
**Main Memory Support:** Yes

Power Management Unit (doze, shutdown, sleep)

Multiple low battery monitoring

Expansion Bus Buffer

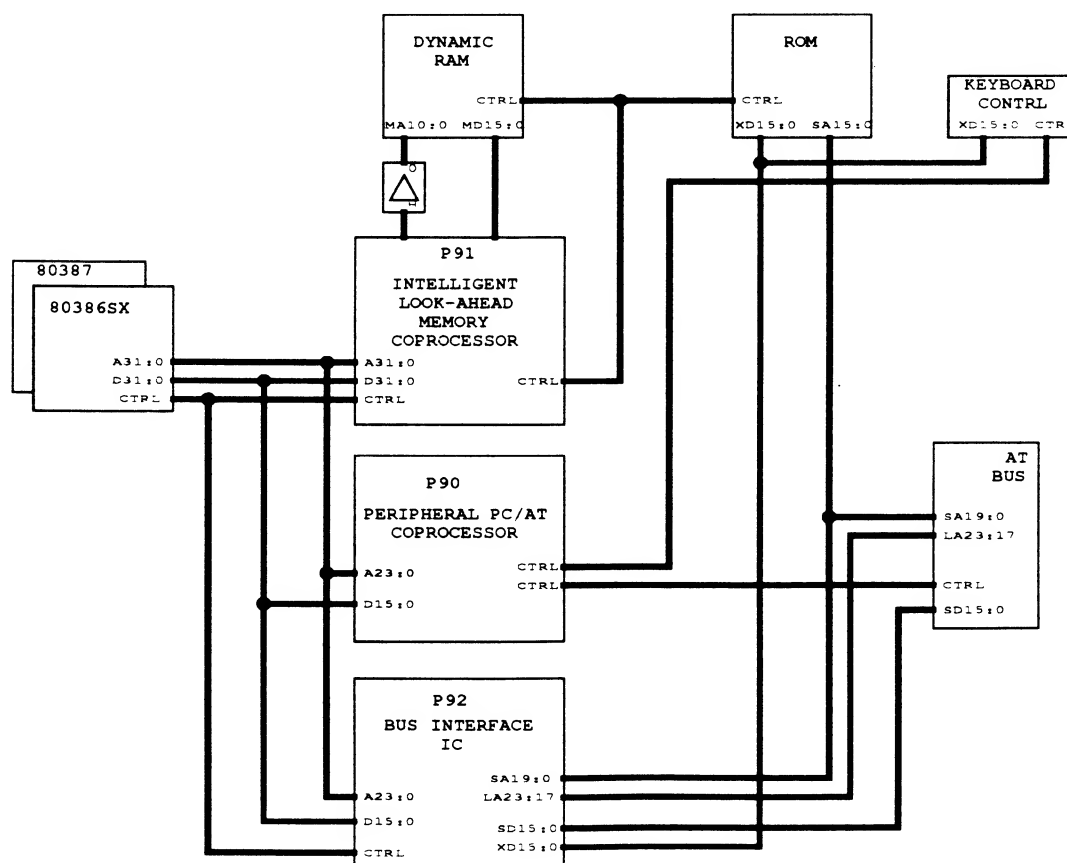
Direct interface to 80386/80387



Appian A90 Notebook Controller







A-19

**Manufacturer:** Appian Technology

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** P92, Single Chip PC AT Expansion Bus Buffer (part of System 90/SX chipset)

**Availability:** 1990

**Second Source:**

**Functions Contained:**

High-speed output diable

Local address latches

System master address to local address redrive logic

**Cache:** No

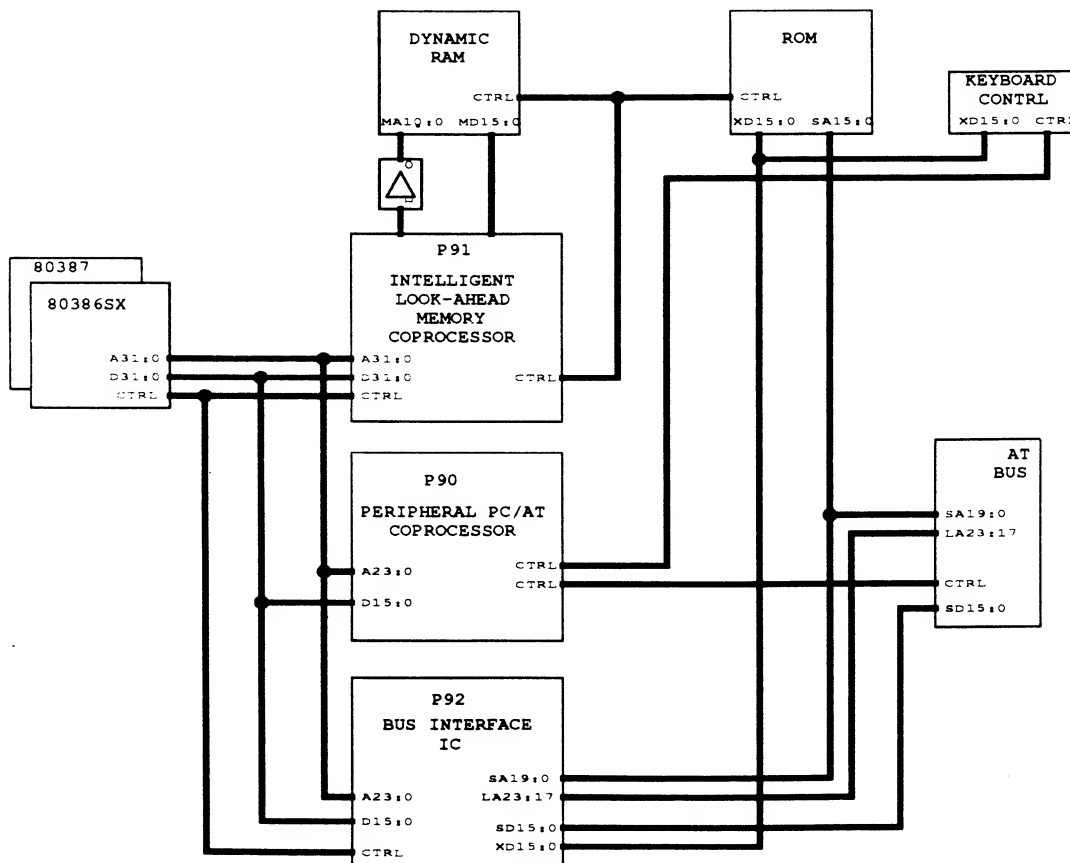
**Clock Speed:** 16, & 20 MHz

**Main Memory Support:** No

High-speed latches and transceivers

Local-to-system bus transceivers

XD bus for ROM & 8042 support



Appian System 90/SX

**Manufacturer:** Appian Technology  
**Processor Supported:** 80386SX/DX  
**System Bus:** AT  
**Part:** P94 PowerMizer, Power Manager Controller  
**Availability:** 1990

**Cache:** No  
**Clock Speed:**  
**Main Memory Support:** No

**Second Source:**

**Functions Contained:**

Supports multiple modes - slow, standby, shutdown, sleep, resume

Supports multiple, independent device power shutdown

(8) power control outputs

Independent programmable time for each mode

Multiple low battery monitoring

CPU & peripheral clock control

Multiple power-on control (keyboard, RTC, etc.)

Refresh support for normal & slow refresh DRAMs

Schematic Not Available At Press Time

**Manufacturer:** Austek

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** A38202, MicroCache

**Availability:** 1991

**Second Source:**

**Functions Contained:**

Supports 16KB, 32KB or 64KB Cache size

Asynchronous snoop bus

Programmable non-cacheable regions

A20 gate support

Pipelined and non-pipelined 80386SX operation

**Cache:** Yes

**Clock Speed:** 25, 33, & 40 MHz

**Main Memory Support:** No

Direct or 2-way set associative mapped memory

ROM caching support

Direct interface to x4, x8 and x16 SRAMS

80387/3187 decode logic

Schematic Not Available At Press Time

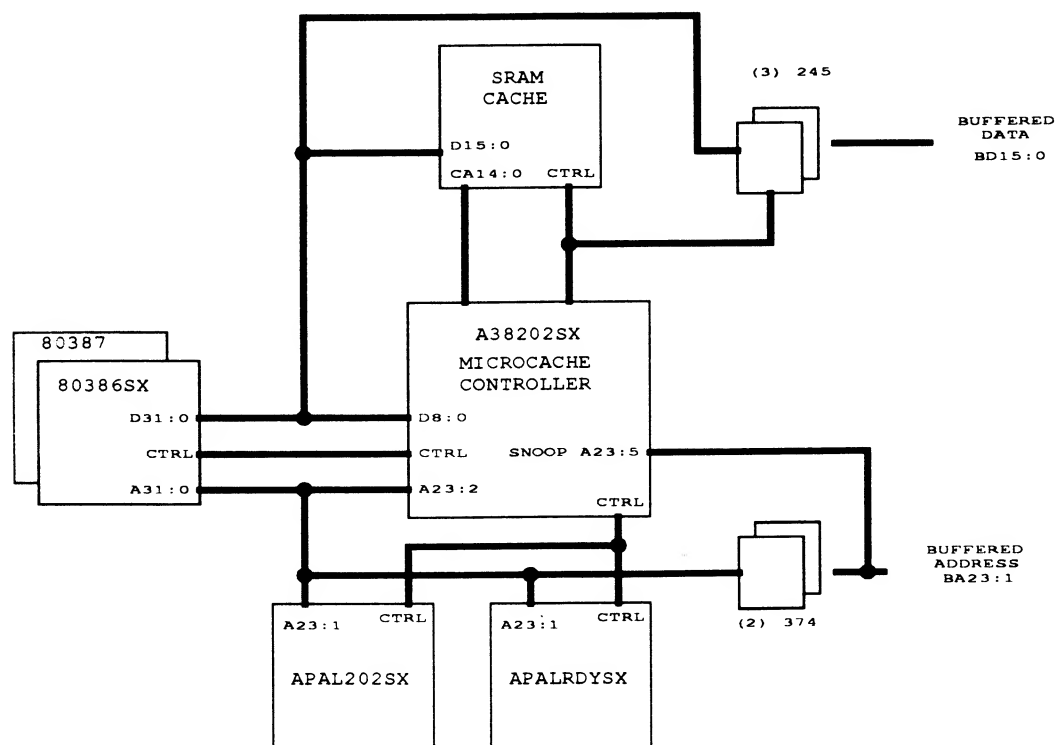
**Manufacturer:** Austek  
**Processor Supported:** 80386SX  
**System Bus:** AT, MCA, EISA  
**Part:** A38202SX, MicroCache  
**Availability:** since 1989  
**Second Source:** none

**Cache:** Yes  
**Clock Speed:** 20, 25 & 33 MHz  
**Main Memory Support:** No

**Functions Contained:**

Supports 16KB, 32KB or 64KB Cache size  
 High performance burst fill  
 Asynchronous snoop bus  
 Direct interface to x4, x8 and x16 SRAMS  
 80387SX decode logic  
 Write through logic

Direct or 2-way set associative mapped memory  
 Least recently used (LRU) replacement algorithm  
 3 programmable non-cacheable regions  
 A20 gate support  
 Pipelined and non-pipelined 80386SX operation  
 Fault detection



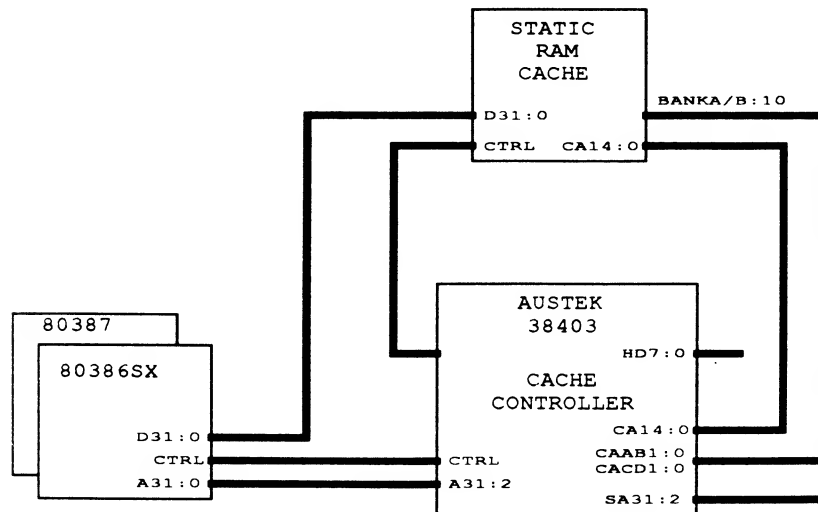
Austek 38202sx "Sidewinder"

**Manufacturer:** Austek  
**Processor Supported:** 80486DX/DX2  
**System Bus:** AT, MCA, EISA  
**Part:** A38403, MicroCache for 486 Systems  
**Availability:** since 1989  
**Second Source:** none  
**Functions Contained:**

**Cache:** Yes  
**Clock Speed:** 25, 33, & 50 MHz  
**Main Memory Support:** No

Supports 128/64K, 128K and 256 KB Cache size	Direct, 2-way or 4-way set associative mapped memory
On-chip 1048 tags	High performance burst fill
Least recently used (LRU) replacement algorithm	Asynchronous snoop bus
multiple programmable non-cacheable regions	Direct interface to x4, x8 and x16 SRAMS
A20 gate support	Write back (forward/write through) cache

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Austek 38403 Cache

**Manufacturer:** Bull Micral (BMA)  
**Processor Supported:** 80386sx  
**System Bus:** Micro Channel Architecture  
**Part:** AZ8031, System Controller  
**Availability:** 1992

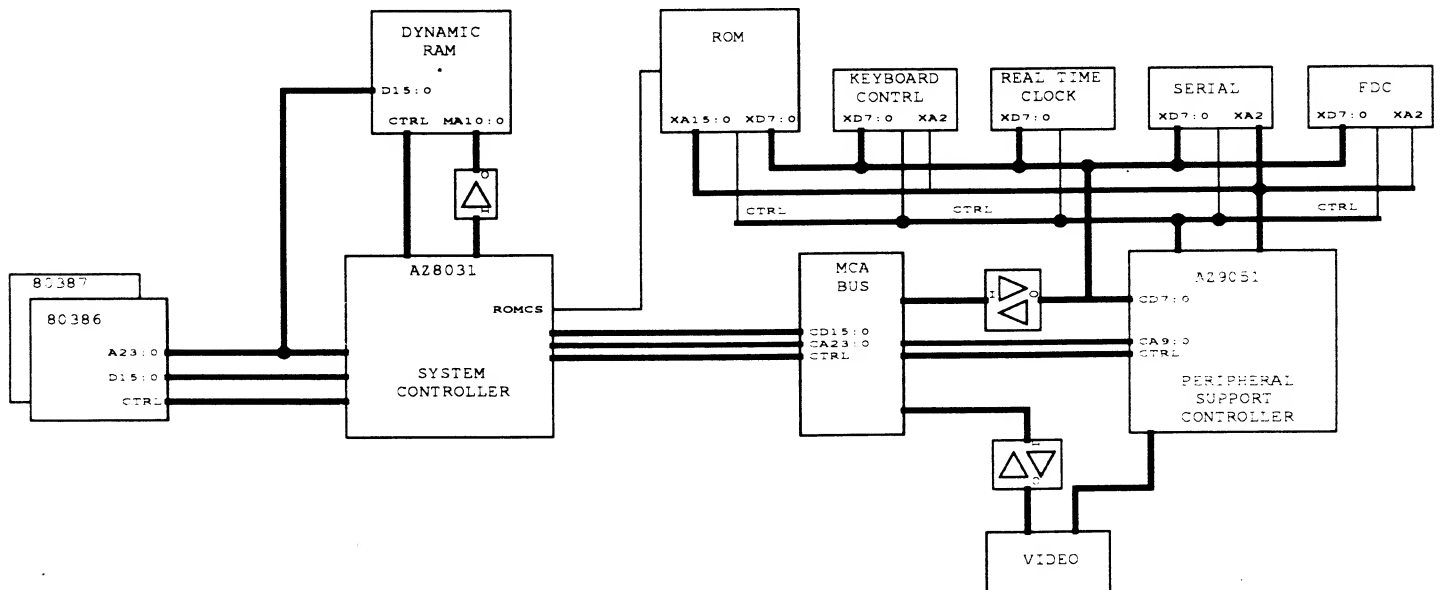
**Second Source:** none

**Functions Contained:**

Provides test features  
 Supports 2-16 MB main memory  
 Provides 8 channel DMA subsystem  
 24-bit address buffer  
 Bidirectional buffer control  
 Self configuring memory controller  
 Programmable DRAM timing - page mode memory controller

**Cache Memory:** No  
**Clock Speed:** 40 MHz  
**Main Memory Support:** Yes

Optimized for 16-bit MCA system  
 Supports 3 banks of 1 MB and 4 MB DRAM  
 Central Arbitration Point (CAP)  
 16-bit data buffer  
 Data & address MUX control



Bull Micral Low Cost 386sx PS/2 Compatible

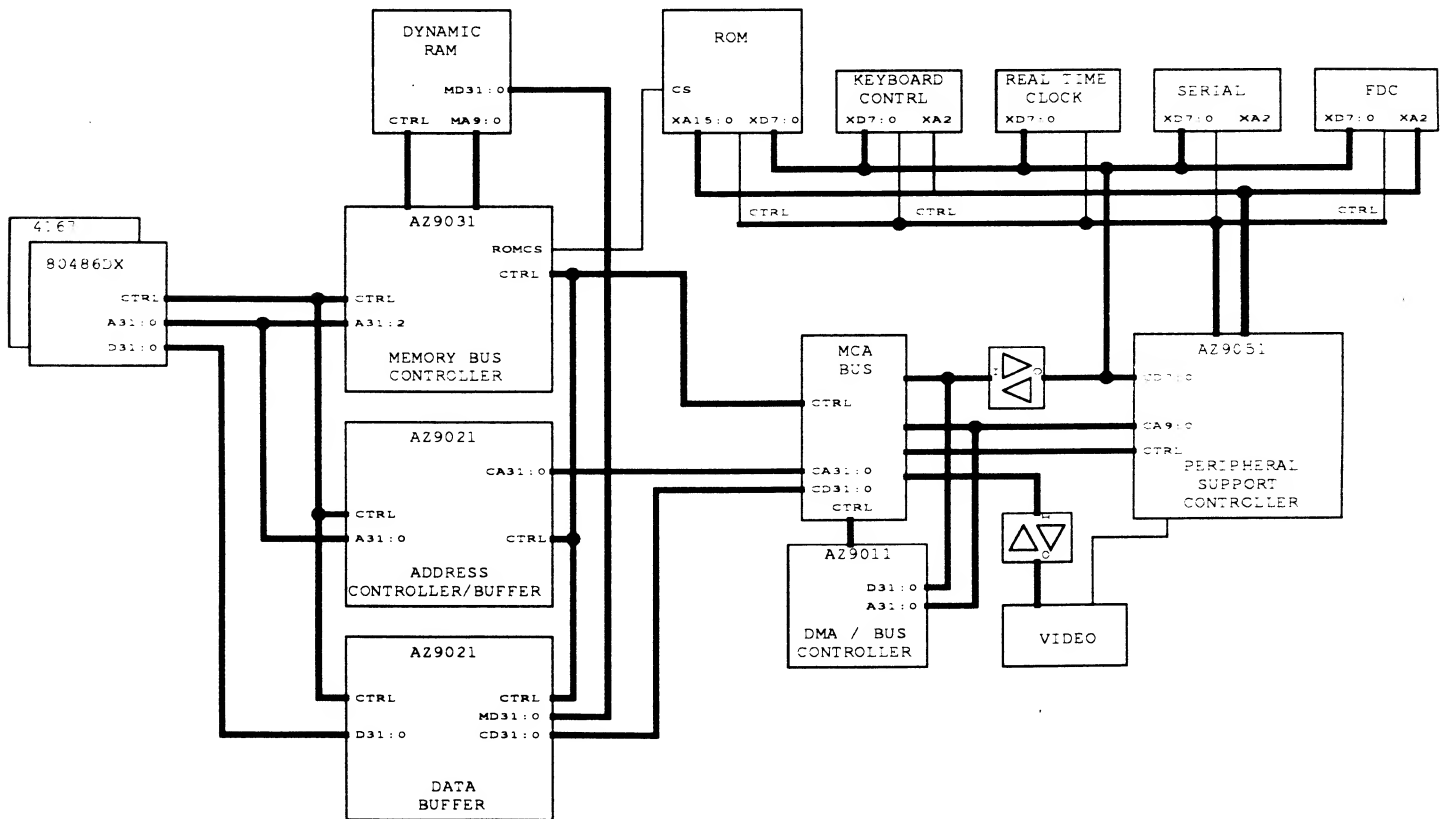
## Personal Computer Design

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**Manufacturer:** Bull Micral (BMA)  
**Processor Supported:**  
**System Bus:** Micro Channel Architecture  
**Part:** AZ9011, Bus Master DMA Controller  
**Availability:** 1991  
**Second Source:** none  
**Functions Contained:**  
(2) 8237 compatible DMA controllers  
Provides bus arbitration  
DRAM refresh logic  
Floppy disk interface  
Bus master crossover logic

---

**Cache Memory:** No  
**Clock Speed:**  
**Main Memory Support:** No



Bull Micral SLIK 486 PS/2 Compatible



**Manufacturer:** Bull Micral (BMA)  
**Processor Supported:**  
**System Bus:** Micro Channel Architecture  
**Part:** AZ9021, Address Buffer/Data Buffer  
**Availability:** 1991

**Cache Memory:** No  
**Clock Speed:**  
**Main Memory Support:** No

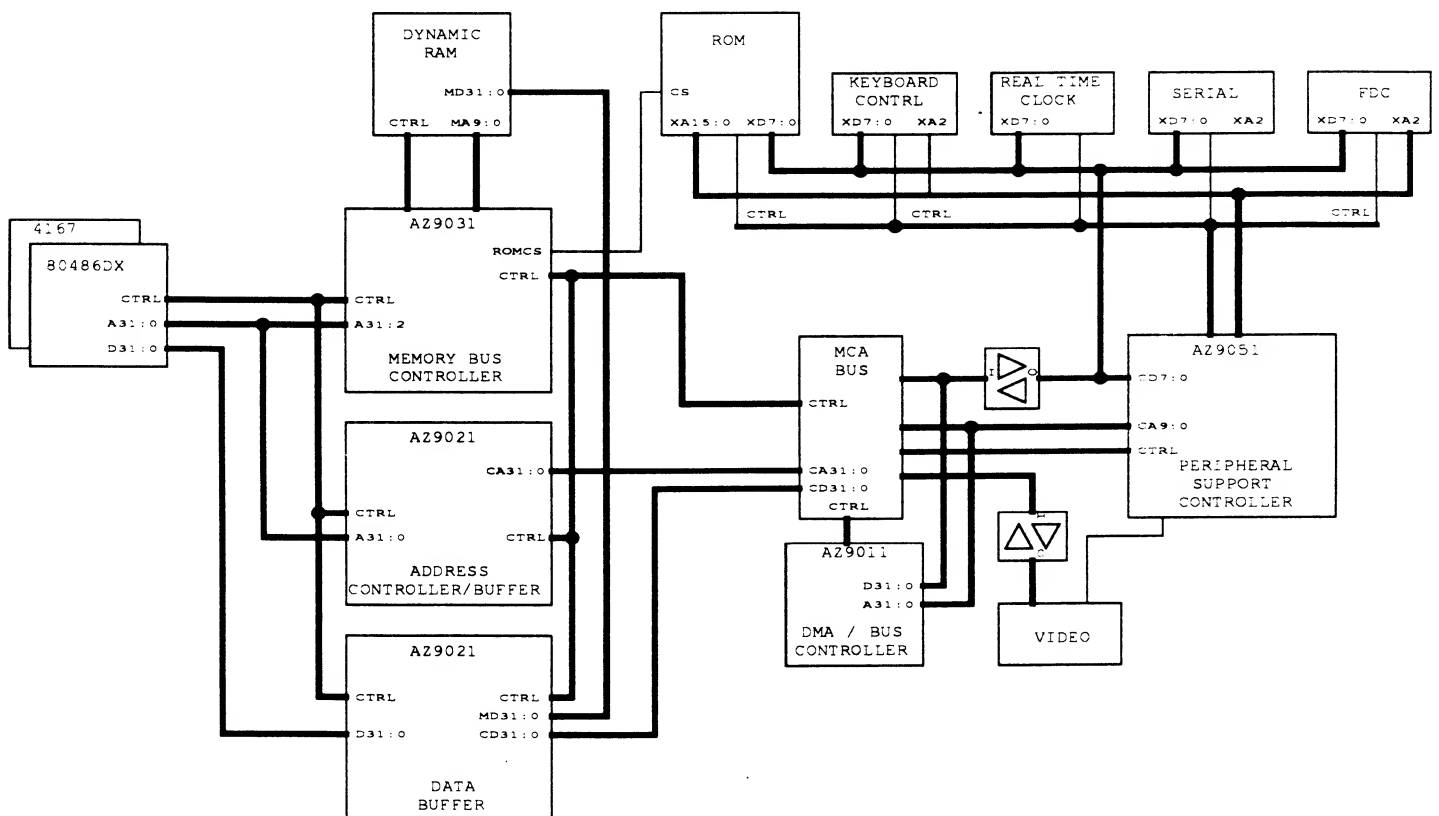
**Second Source:** none

**Functions Contained:**

Translates 8-bit and 16-bit data from MCA bus to 32-bit synchronous SLIK bus

Provides address buffer and latches

Controls flow of addresses among processor, I/O and MCA bus



Bull Micral SLIK 486 PS/2 Compatible

## Personal Computer Design

**Manufacturer:** Bull Micral (BMA)  
**Processor Supported:** 80486  
**System Bus:** Micro Channel Architecture  
**Part:** AZ9022, 64 Bit Data Buffer  
**Availability:** 1991

**Cache Memory:** No  
**Clock Speed:** 50 MHz  
**Main Memory Support:** Yes

**Second Source:** none

**Functions Contained:**

72-bit memory interface (data & parity)

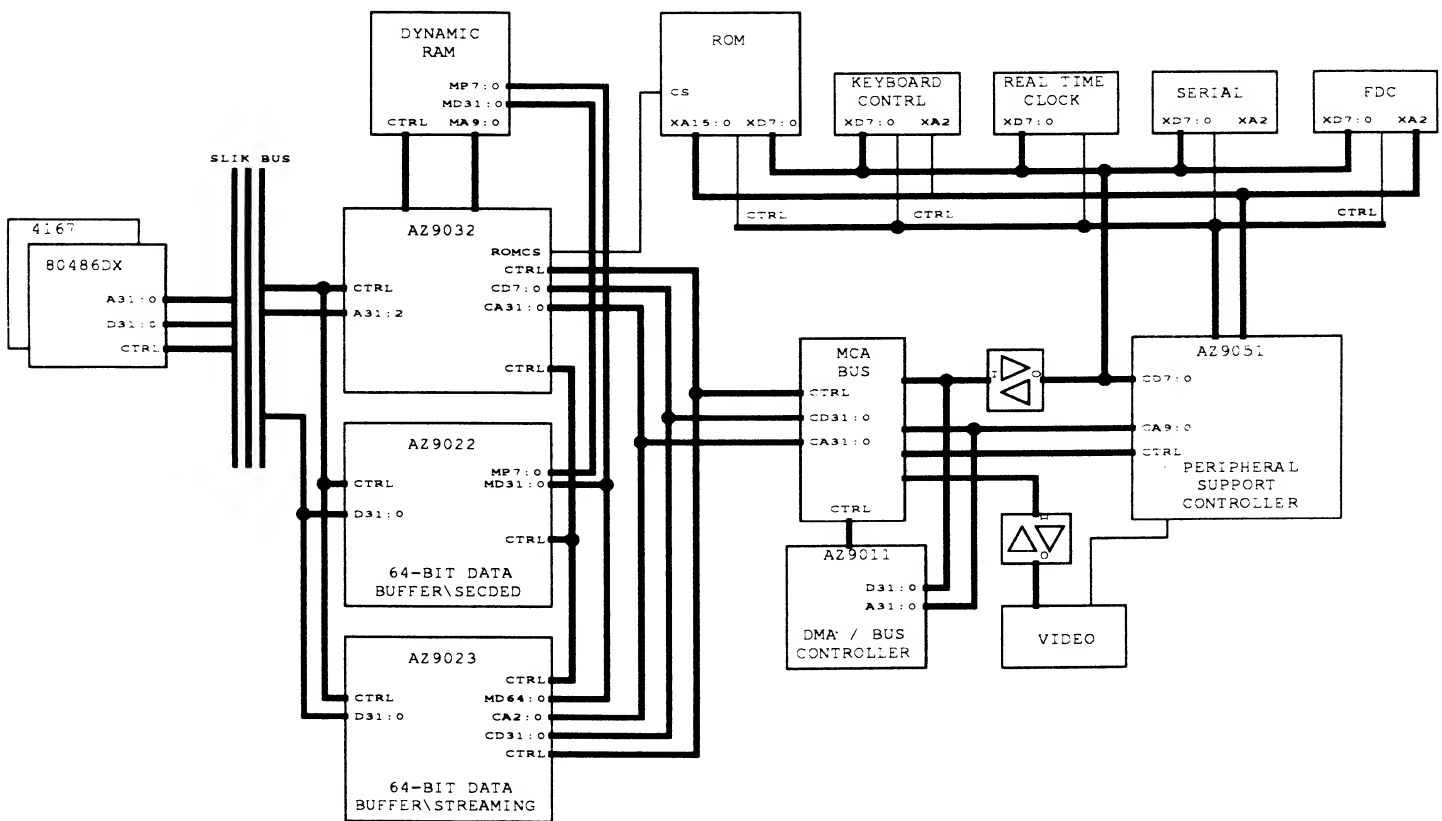
36-bit processor interface

Optional single-bit correction and double-bit error correction (SECDED)

Posts up to 4 processor writes for better throughput

Compatible with 486 and R3000 microprocessors

Performs burst cache line fills to processor or external cache



Bull Micral SLIK 486+

**Manufacturer:** Bull Micral (BMA)  
**Processor Supported:** 80486  
**System Bus:** Micro Channel Architecture  
**Part:** AZ9023, 64 Bit I/O Data Buffer  
**Availability:** 1992

**Cache Memory:** No  
**Clock Speed:** 50 MHz  
**Main Memory Support:** Yes

**Second Source:** none

**Functions Contained:**

72-bit memory interface (data & parity)

36-bit processor interface

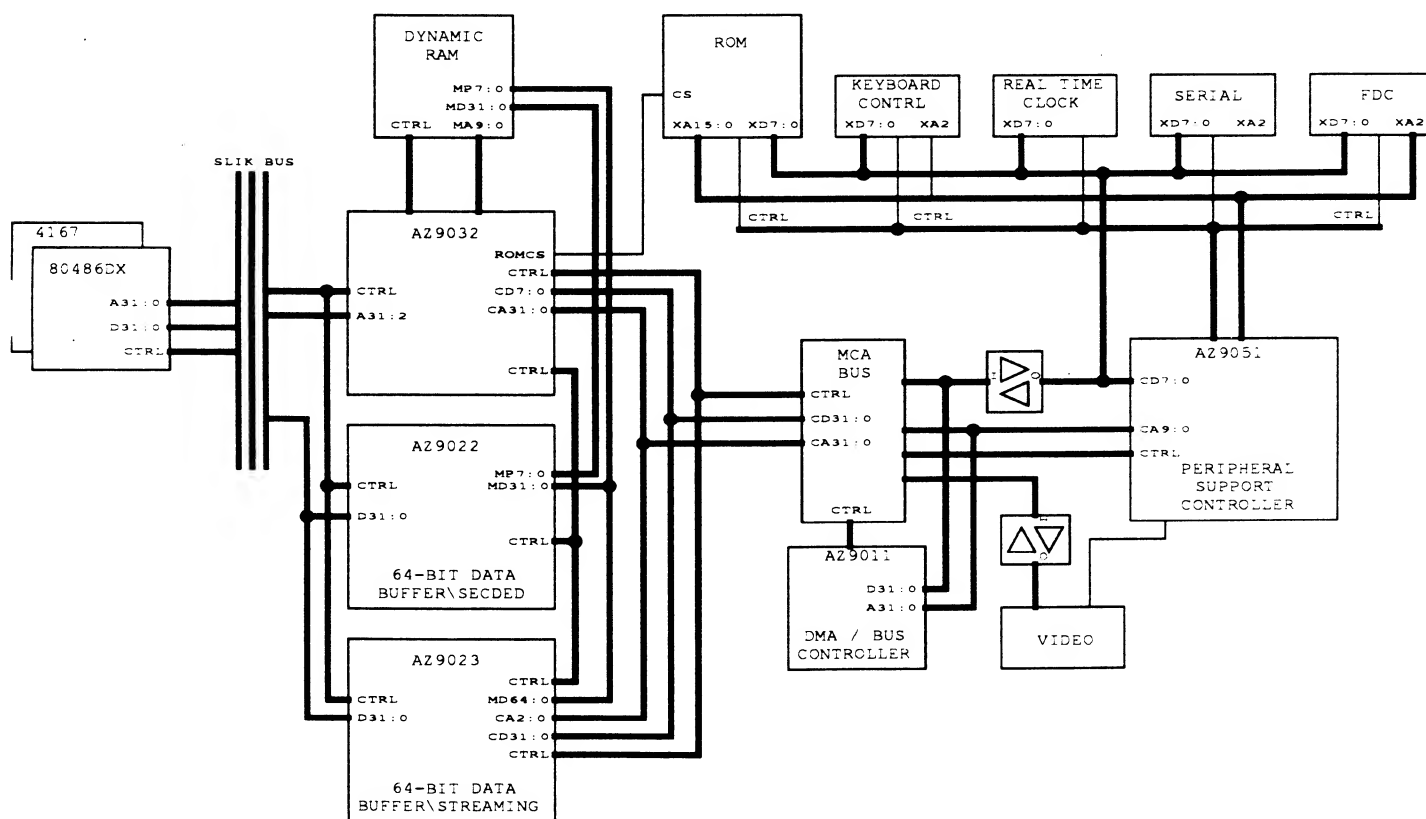
Optional single-bit correction and double-bit error correction (SECDED)

Micro Channel data streaming up to 40 MB per second

Micro Channel data parity

Operates in conjunction with AZ9022 @ 50 MHz

Optionally performs central translator function for MCA data and parity



Bull Micral SLIK 486+

**Manufacturer:** Bull Micral (BMA)  
**Processor Supported:** 80486  
**System Bus:** Micro Channel Architecture  
**Part:** AZ9031, Memory/Bus Controller  
**Availability:** 1991

**Second Source:** none

**Functions Contained:**

Supports four banks of 1M x 1 DRAMs

Supports 16 MB main memory

Supports 4K byte pages

Provides address multiplexing

Memory access between CPU & main memory (Synchronous state machine)

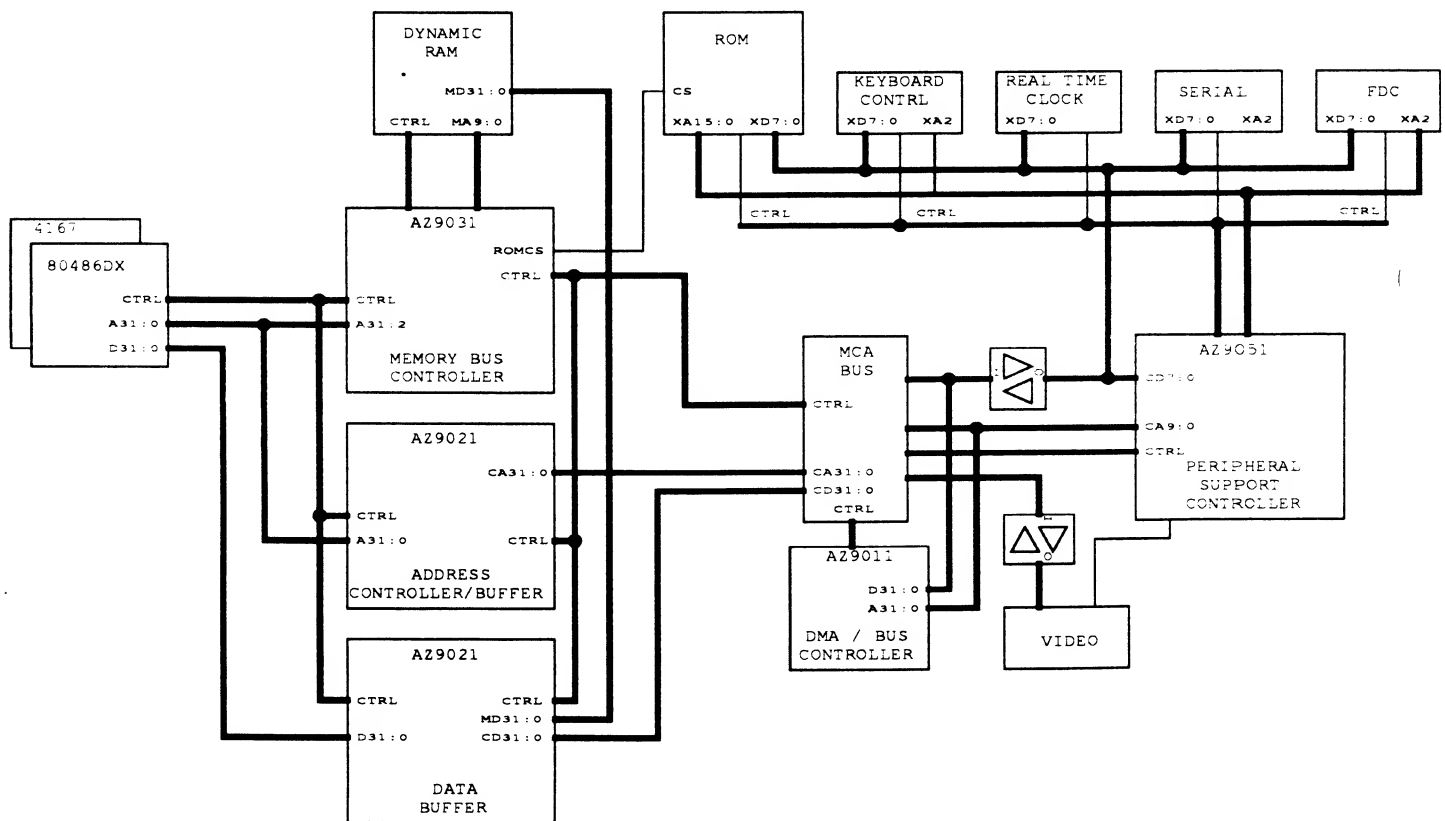
Asynchronous DRAM controller (MCA & main memory)

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**Cache Memory:** No

**Clock Speed:** 25 & 33 MHz

**Main Memory Support:** Yes



Bull Micral SLIK 486 PS/2 Compatible

**Manufacturer:** Bull Micral (BMA)  
**Processor Supported:** 80486  
**System Bus:** Micro Channel Architecture  
**Part:** AZ9032, Memory/Bus Controller  
**Availability:** 1992

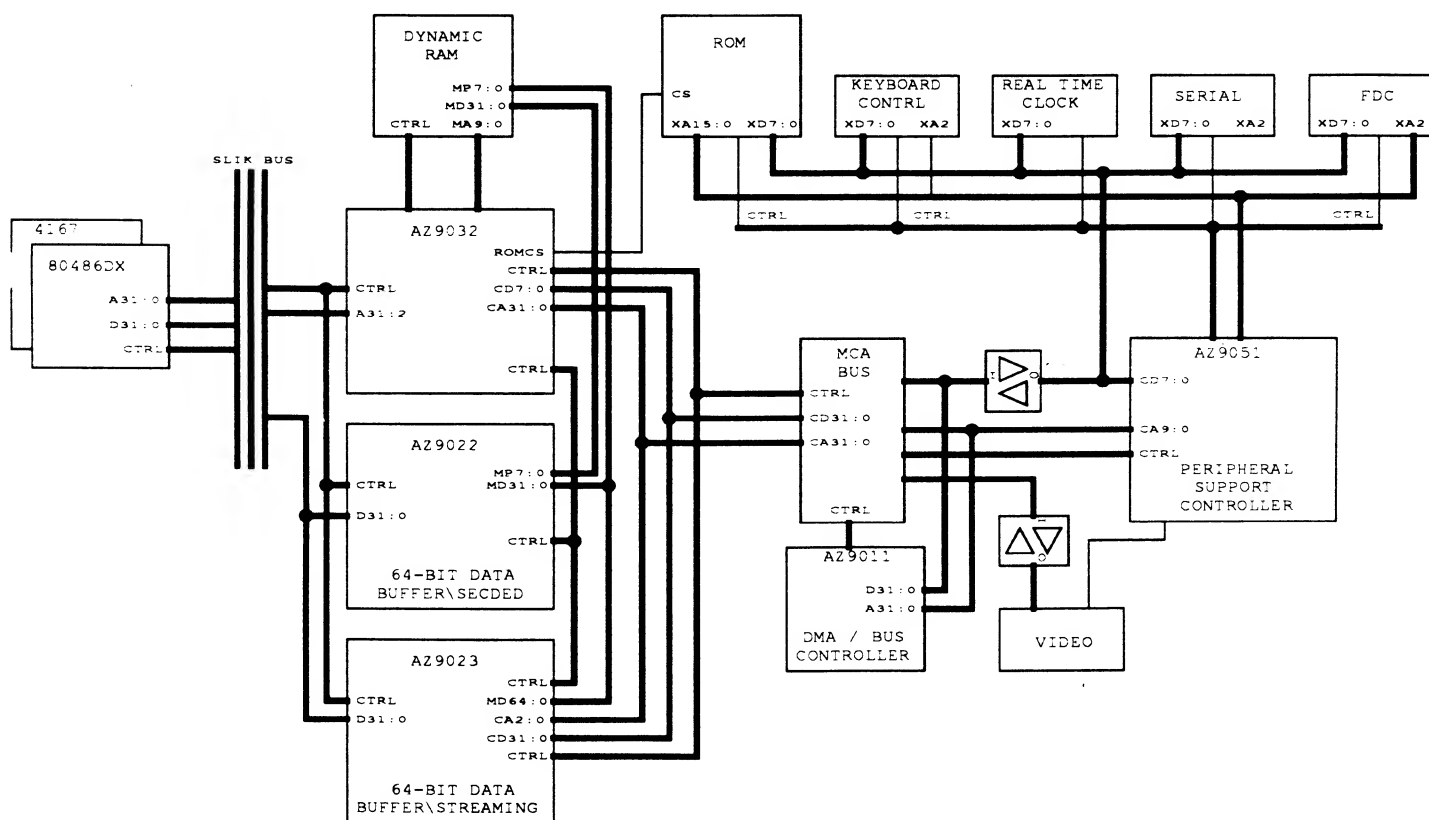
**Second Source:** none

**Functions Contained:**

Supports 2 to 64 MB, page mode main memory  
 Provides 64-bit memory bus  
 Secondary cache support  
 Optional SECDED error correction  
 Full 24mA Address and Data Buffers  
 Memory write buffers 4 deep  
 Data/Address parity support on MCA bus

**Cache Memory:** Yes  
**Clock Speed:** 50 MHz  
**Main Memory Support:** Yes

Supports 1MB and 4MB DRAMs  
 Programmable memory state machines  
 Supports posted, buffered writes  
 MCA compatible  
 Supports 50 MHz 486 burst mode  
 40 MB per second MCA transfers  
 Dual port memory controller



Bull Micral SLIK 486+

**Manufacturer:** Bull Micral (BMA)

**Processor Supported:**

**System Bus:** Micro Channel Architecture

**Part:** AZ9051, Peripheral Support Chip

**Availability:** 1991

**Second Source:** none

**Functions Contained:**

Interrupt controller subsystem

Counter/timer subsystem

Parallel printer port subsystem

Option- and hardware-configuration subsystem

Address decoding

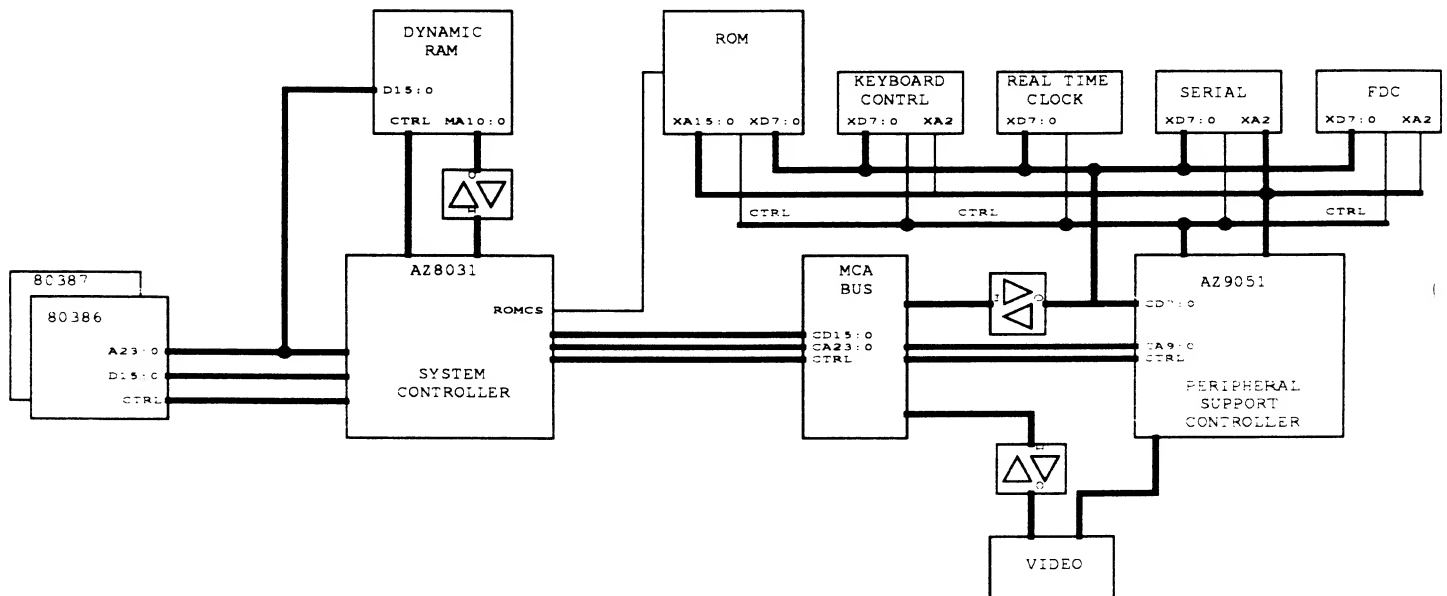
Bus control functions

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**Cache Memory:** No

**Clock Speed:**

**Main Memory Support:** No



Bull Micral Low Cost 386sx PS/2 Compatible

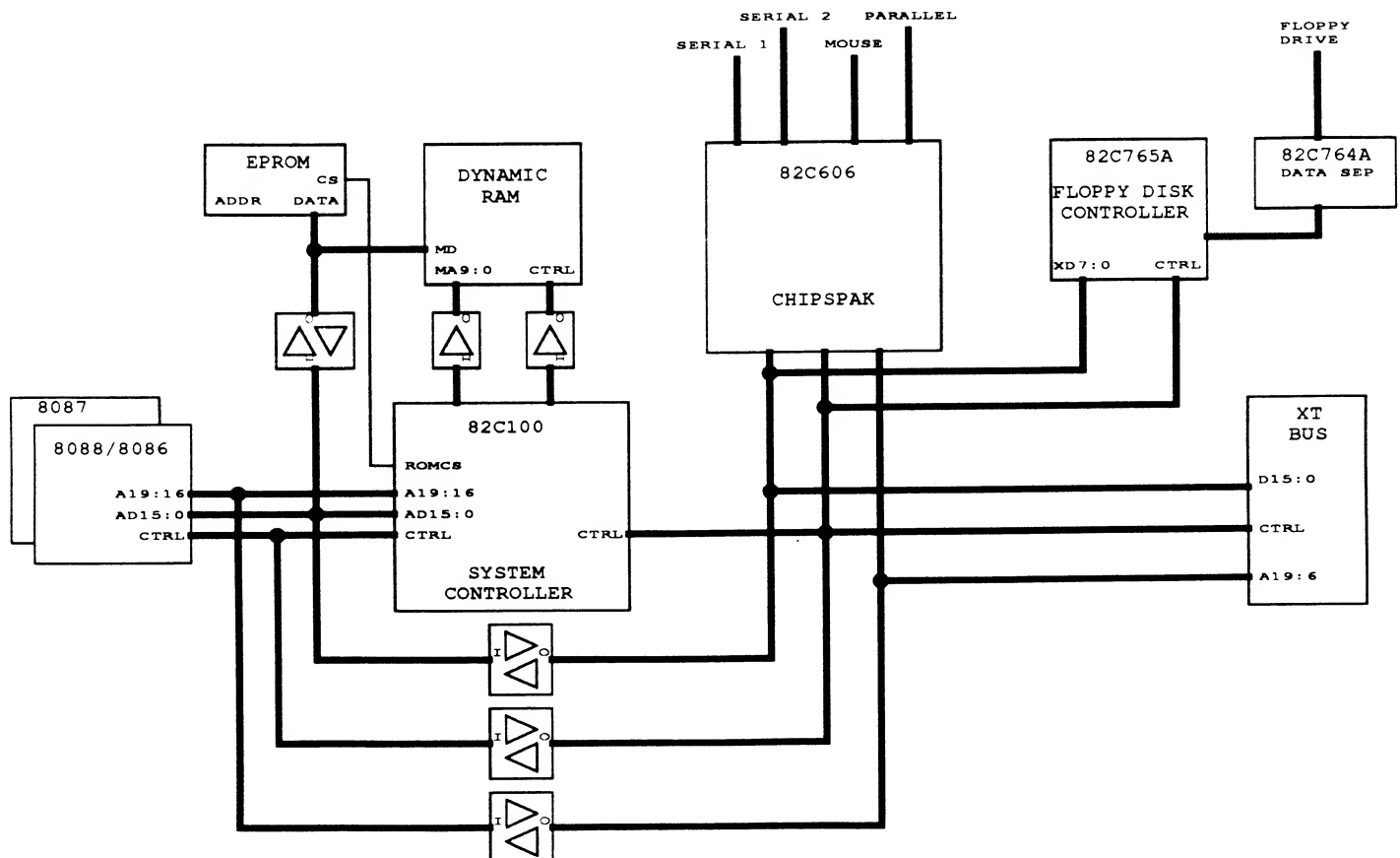
**Manufacturer:** Chips & Technologies  
**Processor Supported:** 8086/8088, V30/V20  
**System Bus:** XT  
**Part:** 82C100, IBM PS/2 Model 30 and Super XT Compatible Chip  
**Availability:** 1988

**Cache:** No  
**Clock Speed:** 10 MHz  
**Main Memory:** Yes

**Second Source:** none

**Functions Contained:**

8284 compatible clock generator	8288 compatible bus controller
8237 compatible DMA controller	8259 compatible interrupt controller
8254 compatible programmable interval timer/counter	8255 compatible peripheral I/O
Supports 2.5 MB DRAM (zero wait state, 2 banks + EMS)	Provides ROM chip select
Supports 64K, 256K and 1M bit DRAMs (and SRAMs)	Allows programmable wait states
Provides parity generation/checking	Provides configuration registers
Provides 16-bit to 8-bit conversion	Supports LIM EMS 4.0
Provides power management with sleep, suspend & resume modes	



## Personal Computer Design

**Manufacturer:** Chips & Technologies

**Processor Supported:** 8088, V20

**System Bus:** XT

**Part:** 82C101, IBM PS/2 Model 30 and Super XT Compatible Chip

**Availability:** 1988

**Second Source:** none

**Functions Contained:**

8284 compatible clock generator

8237 compatible DMA controller

8254 compatible programmable interval timer/counter

Supports 2.5 MB DRAM (zero wait state, 2 banks + EMS)

Supports 64K, 256K and 1M bit DRAMs

Provides parity generation/checking

Provides 16-bit to 8-bit conversion

**Cache:** No

**Clock Speed:** 10 MHz

**Main Memory:** Yes

8288 compatible bus controller

8259 compatible interrupt controller

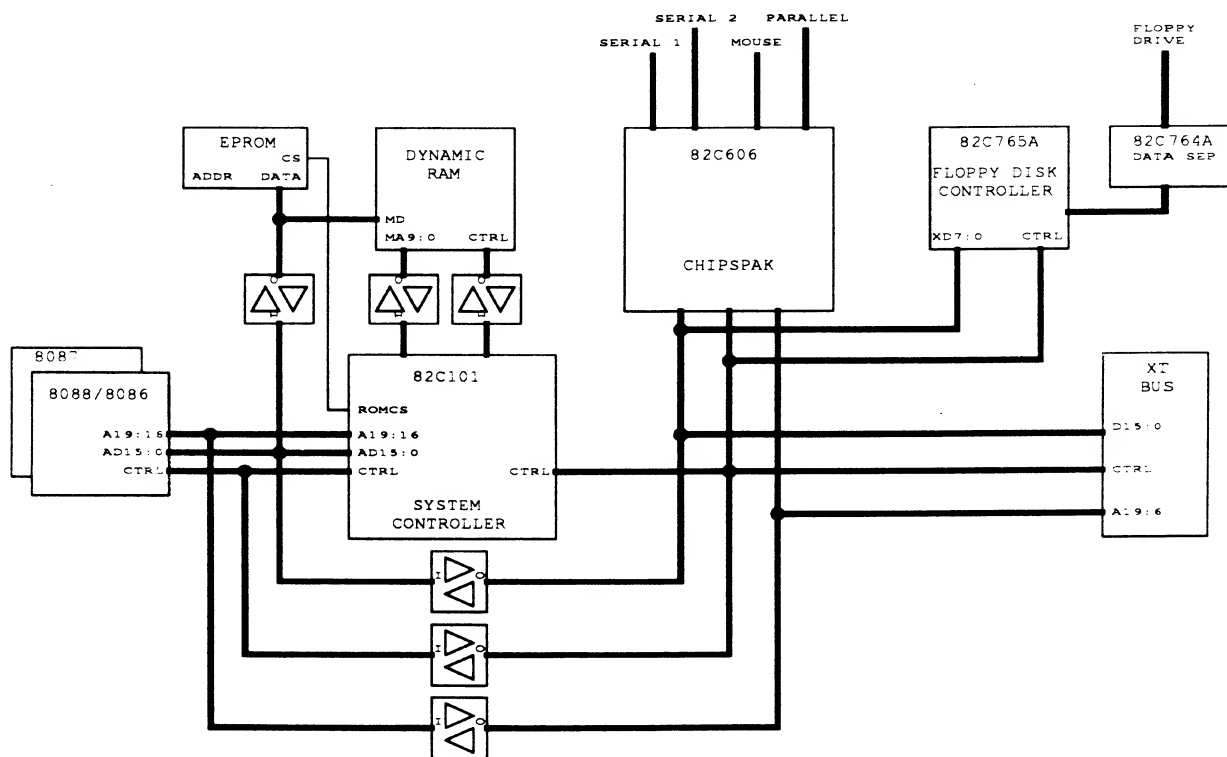
8255 compatible peripheral I/O

Provides ROM chip select

Allows programmable wait states

Provides configuration registers

Supports LIM EMS 4.0



IBM PS/2 MODEL 30 & SUPER XT Compatible Chip (82C101)



**Manufacturer:** Chips & Technologies  
**Processor Supported:** 8086/8088, V30/V20  
**System Bus:** XT  
**Part:** 82C110, IBM PS/2 Model 30 and Super XT Compatible Chip  
**Availability:** 1990

**Cache:** No  
**Clock Speed:** 10 MHz  
**Main Memory:** Yes

**Second Source:** none

**Functions Contained:**

- (1) 8284 compatible clock generator
- (1) 8237 compatible DMA controller
- (1) 8254 compatible timer/counter

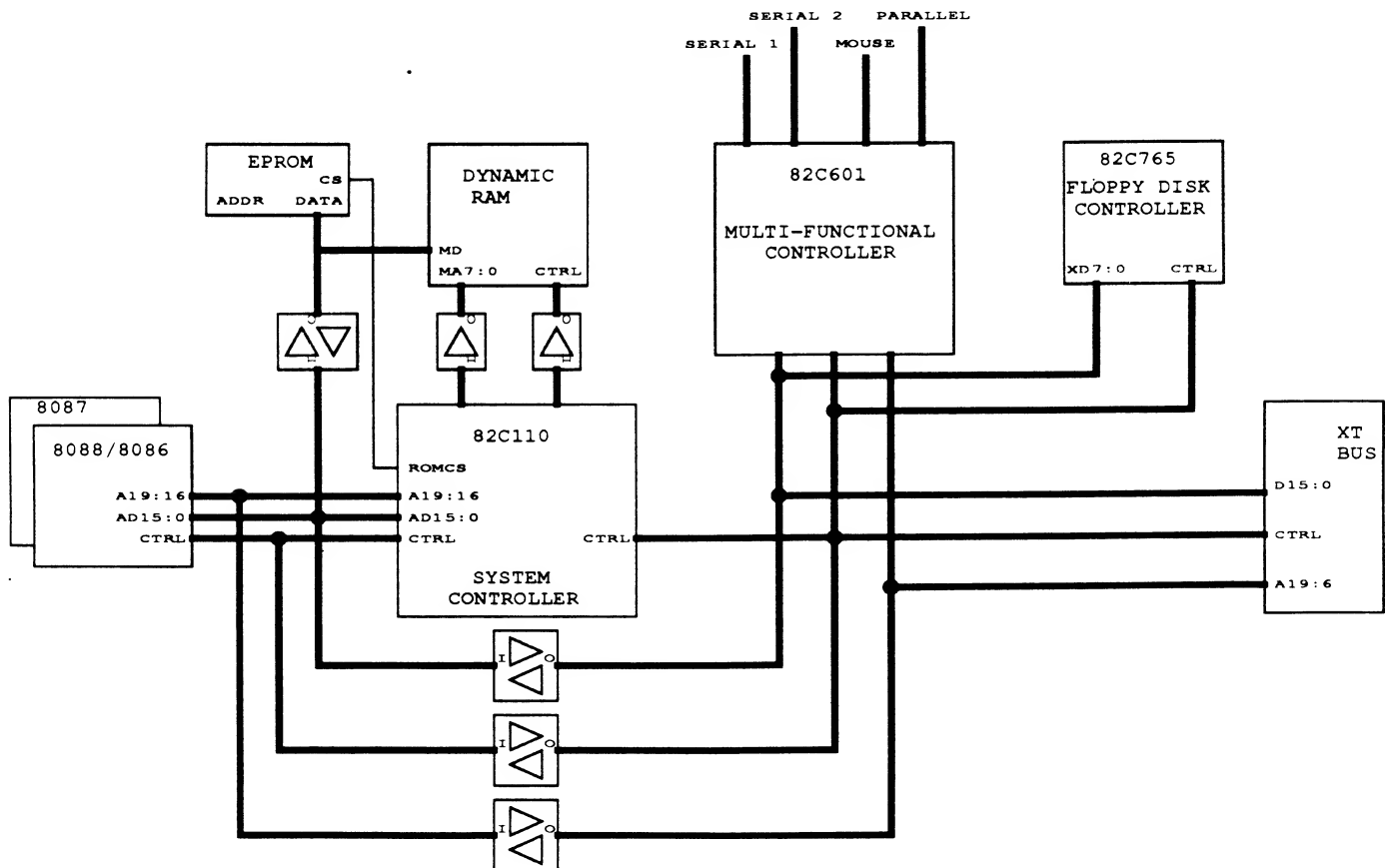
Provides ROM chip select

Provides parity generation/checking

Supports LIM EMS 4.0

Supports 2.5 MB DRAM (zero wait state, 2 banks + EMS)

- (1) 8288 compatible bus controller
  - (1) 8259 compatible interrupt controller
  - (1) 8255 compatible peripheral I/O
- Supports 64K, 256K and 1M bit DRAMs  
 Provides configuration registers



IBM PS/2 MODEL 30 & SUPER XT Compatible Chip

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C201, System Control Chip (part of CS8220 PC/AT Compatible Chipset)

**Availability:** 1986

**Second Source:** none

**Functions Contained:**

Contains clock generation and reset/ready circuitry

Command and control signal generation (MEMR, MEMW, etc)

Conversion logic (16-bit data to 8-bit for external devices)

Contains wait state logic

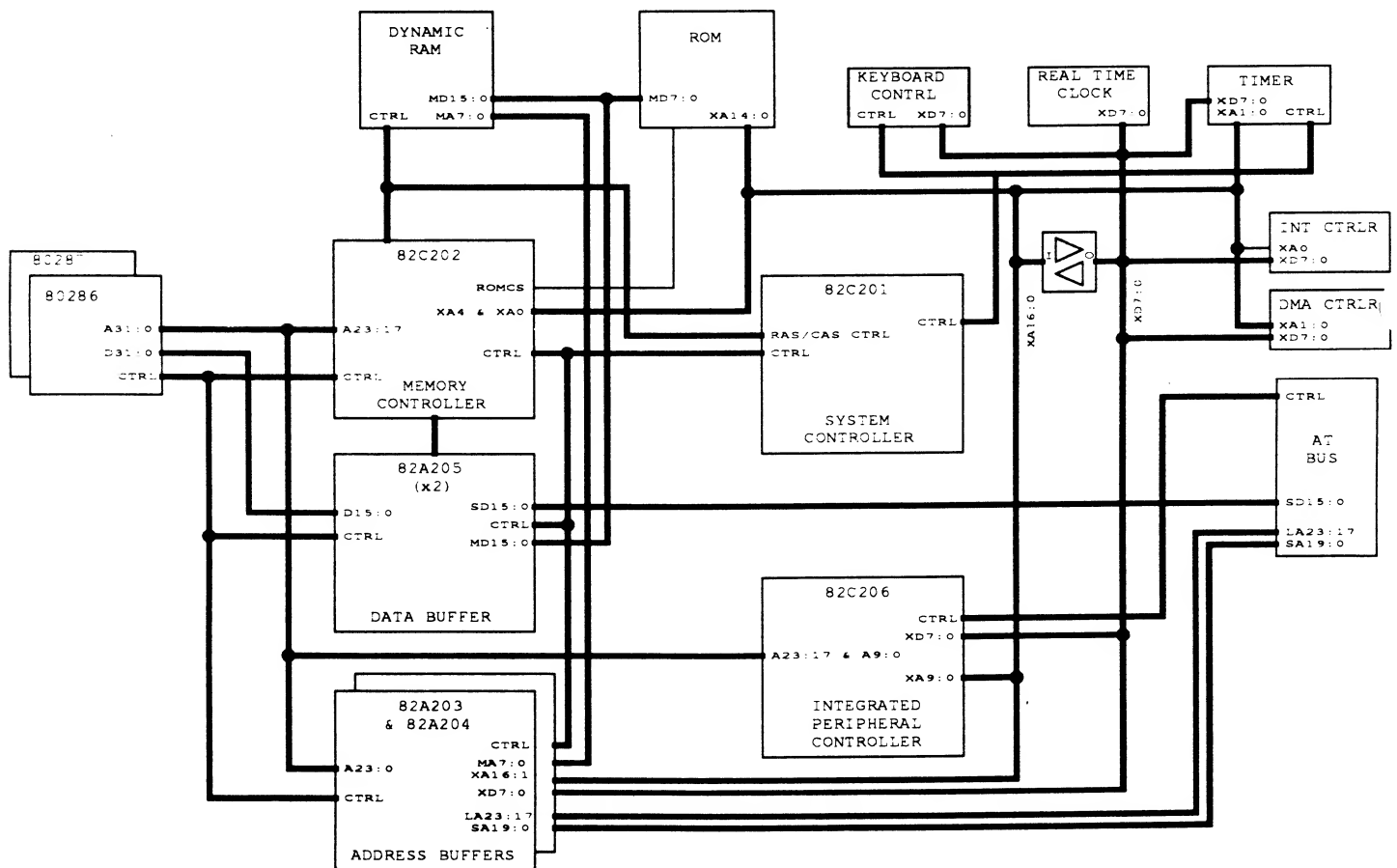
DMA and refresh

NMI and error logic

**Cache:** No

**Clock Speed:** 8 or 10 MHz

**Main Memory:** No



CS8220 Chips & Tech PC/AT Compatible Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C202, RAM/ROM Decode I/O Control (part of CS8220 PC/AT Compatible Chipset)

**Availability:** 1986

**Second Source:** none

**Functions Contained:**

Supports 8 or 10 MHz (1 wait state) or 6 MHz (zero wait states)

Supports 64K and 256K DRAMs (in mixed mode)

Supports up to 1MB on-board memory

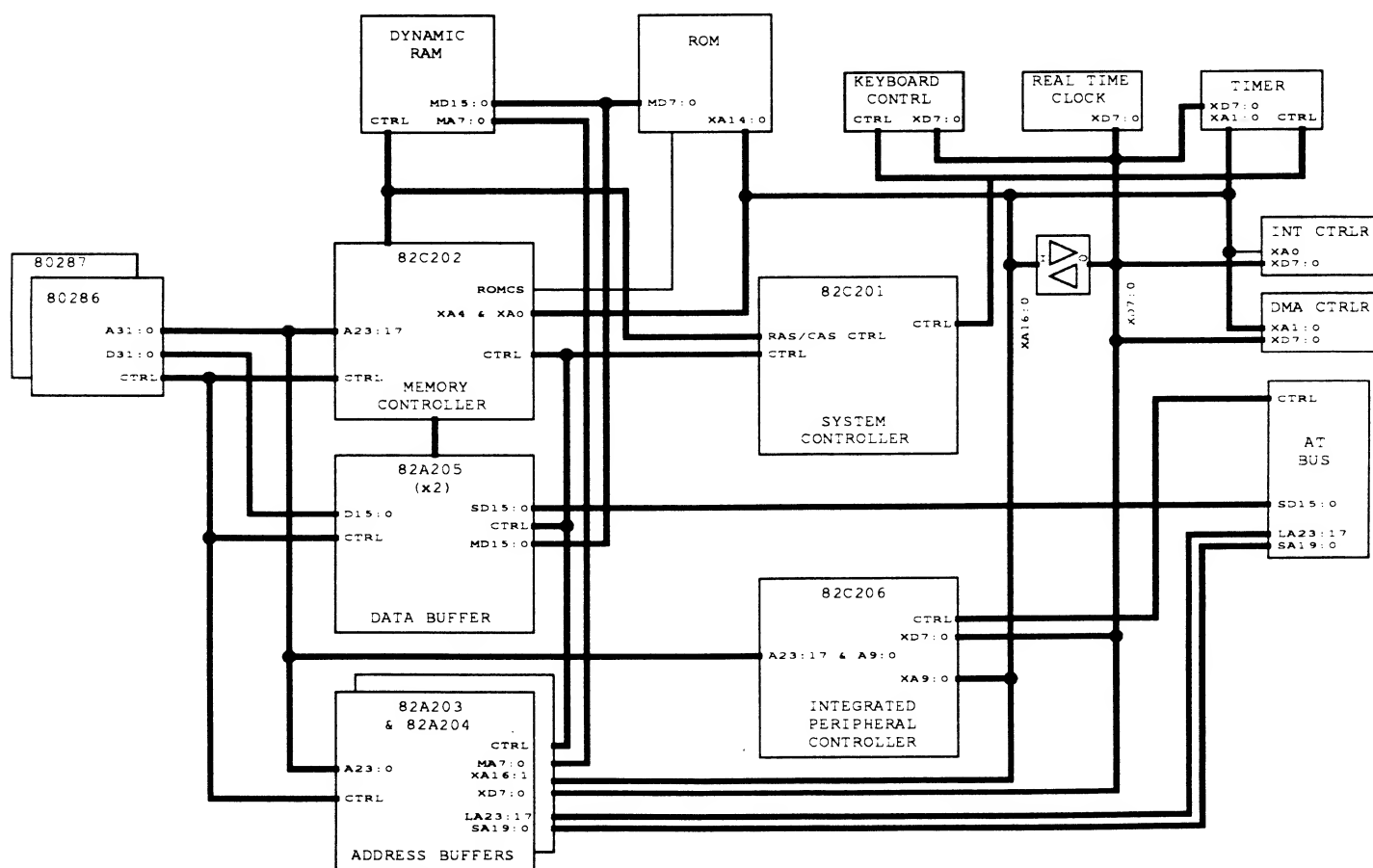
Provides parity error detection circuitry

Provide control signals for clock/calendar, status/control port, NMI and the keyboard controller

**Cache:** No

**Clock Speed:** 8 or 10 MHz

**Main Memory:** Yes

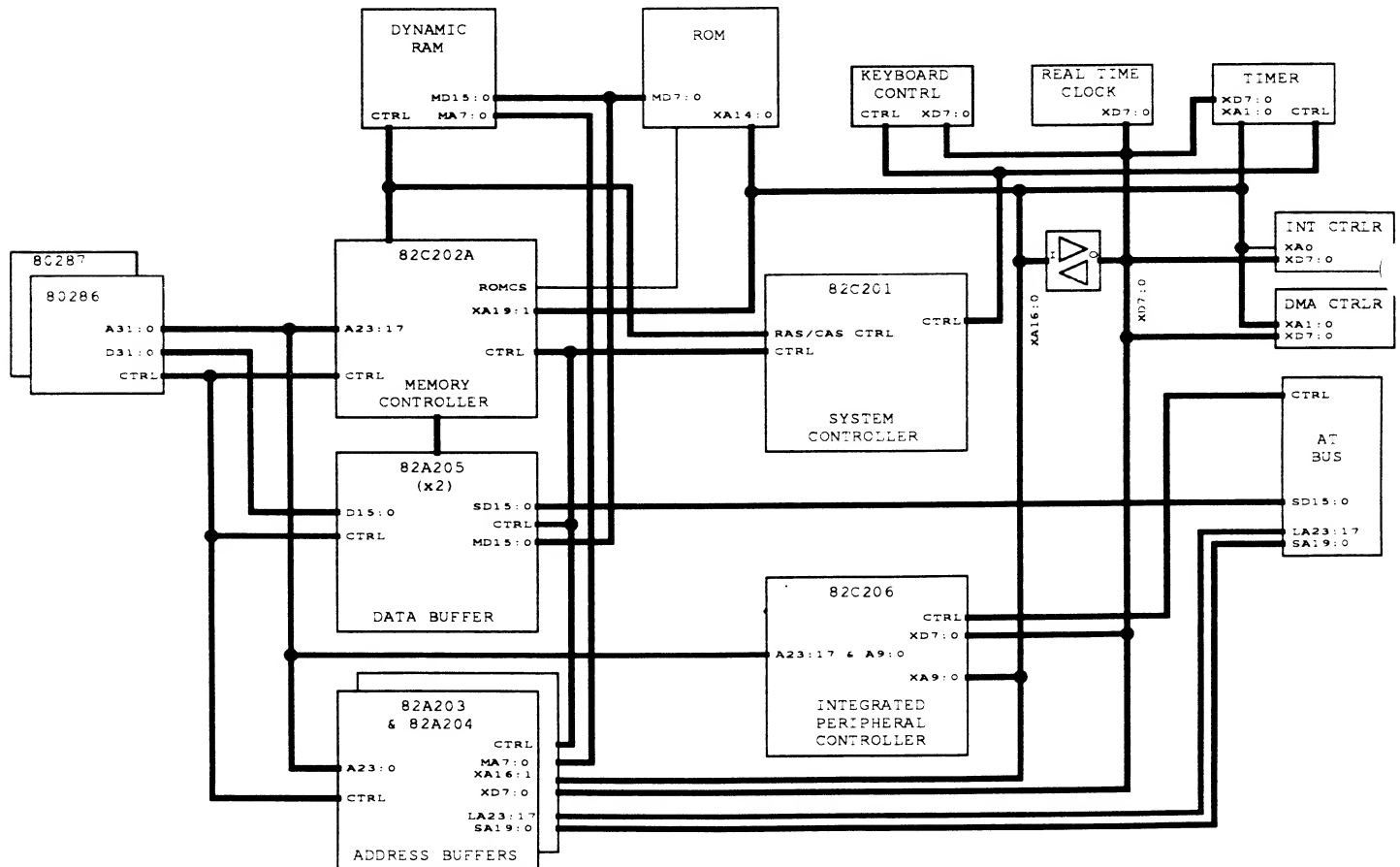


CS8220 Chips & Tech PC/AT Compatible Chipset

**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80286  
**System Bus:** AT  
**Part:** 82C202A, Advanced Memory Controller  
**Availability:** 1986  
**Second Source:** none  
**Functions Contained:**

**Cache:** No  
**Clock Speed:** 10 & 12.5 MHz  
**Main Memory:** Yes

Super set of 82C202 Memory Controller for CS8220 based PC/AT  
Synchronous switching between two user defined clock inputs  
Supports 256K and 1M bit DRAMs  
Options for dividing I/O channel clock and DMA clock by two (10 & 12.5 MHz)  
Supports memory configurations from 1M to 4MB  
Supports remapping of upper 384K to top of memory



CS8220 Chips & Tech PC/AT Compatible Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C203, High Address Bus Buffer & Port B Chip (part of CS8220 PC/AT Compatible Chipset)

**Availability:** 1986

**Second Source:** none

**Functions Contained:**

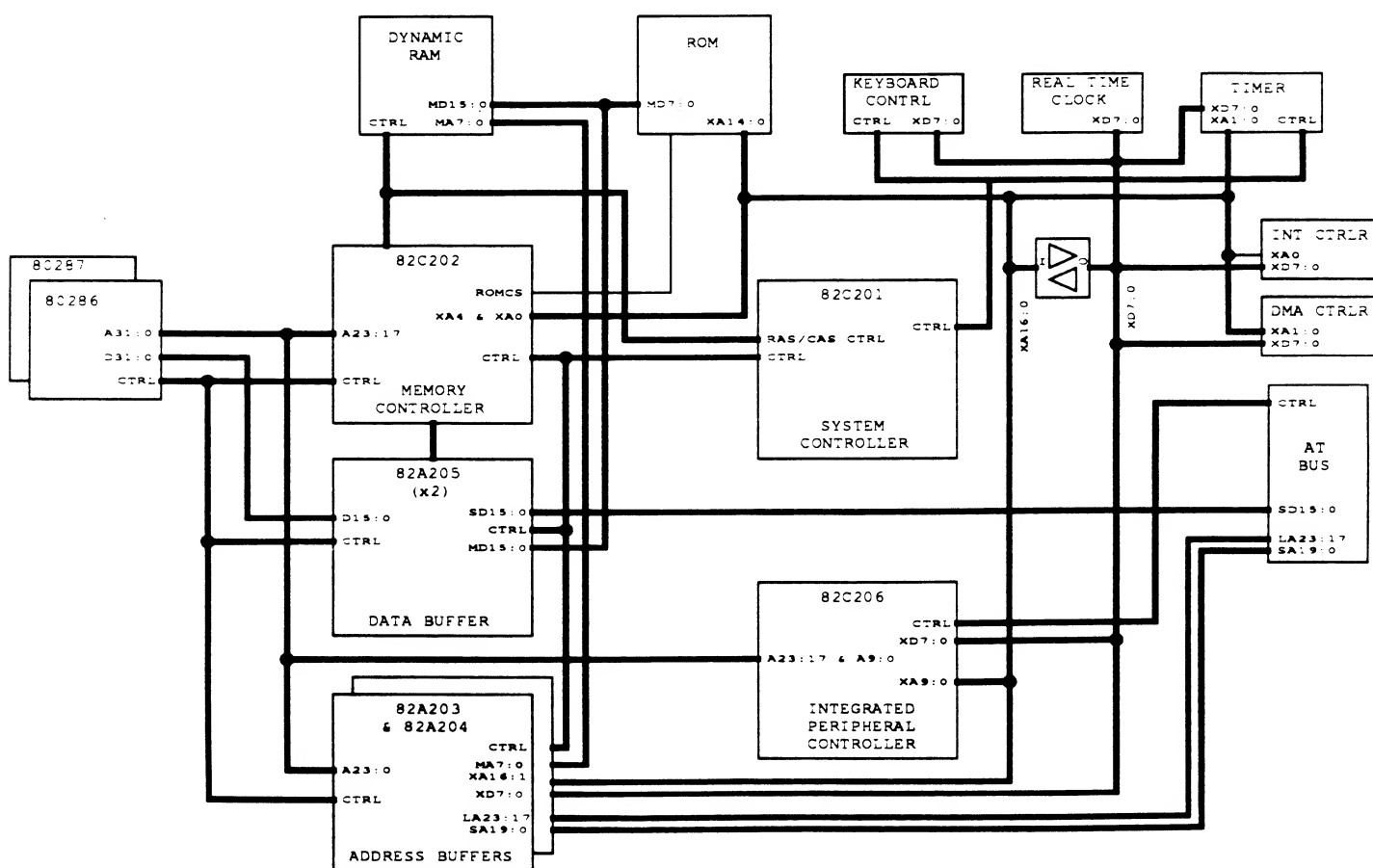
Provides drives & buffers for CPU, System & Local I/O control

Provides buffer capability for high address bus (A17-A23)

**Cache:** No

**Clock Speed:** 8 or 10 MHz

**Main Memory:** No



CS8220 Chips & Tech PC/AT Compatible Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C204, Low Address Bus Buffer & Refresh Counter (part of CS8220 PC/AT Compatible Chipset)

**Availability:** 1986

**Second Source:** none

**Functions Contained:**

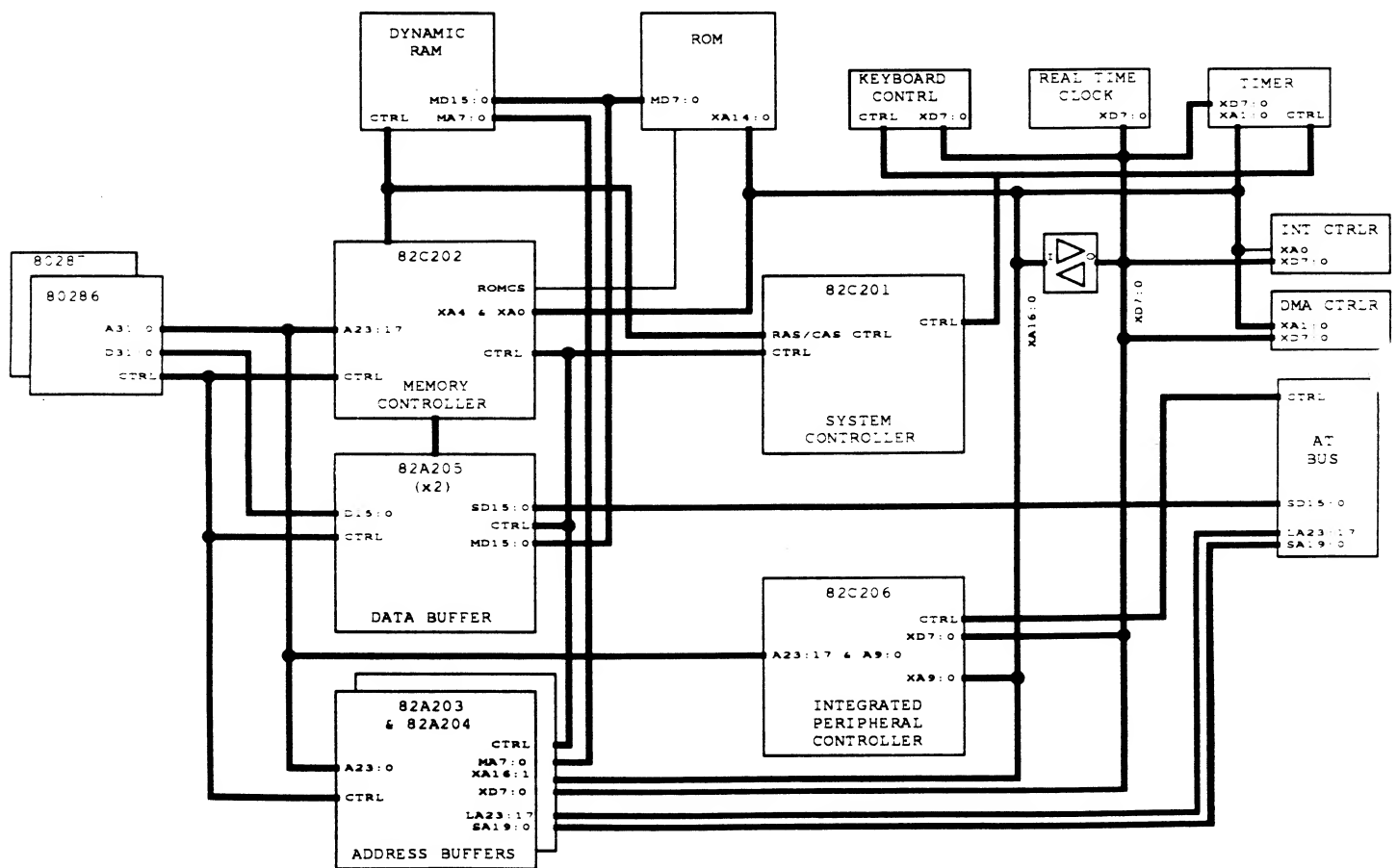
Provides buffer capability for lower address bus (A0-A16)

Provides drivers for memory address bus (MA0-MA7)

**Cache:** No

**Clock Speed:** 8 or 10 MHz

**Main Memory:** No



CS8220 Chips & Tech PC/AT Compatible Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C205, Data Bus Buffer & Parity Generation Chip (part of CS8220 PC/AT Compatible Chipset)

**Availability:** 1986

**Second Source:** none

**Functions Contained:**

Provides data bus buffers and drivers for CPU (D0-D15), System (SD0-SD15) and Memory (MD0-MD15)

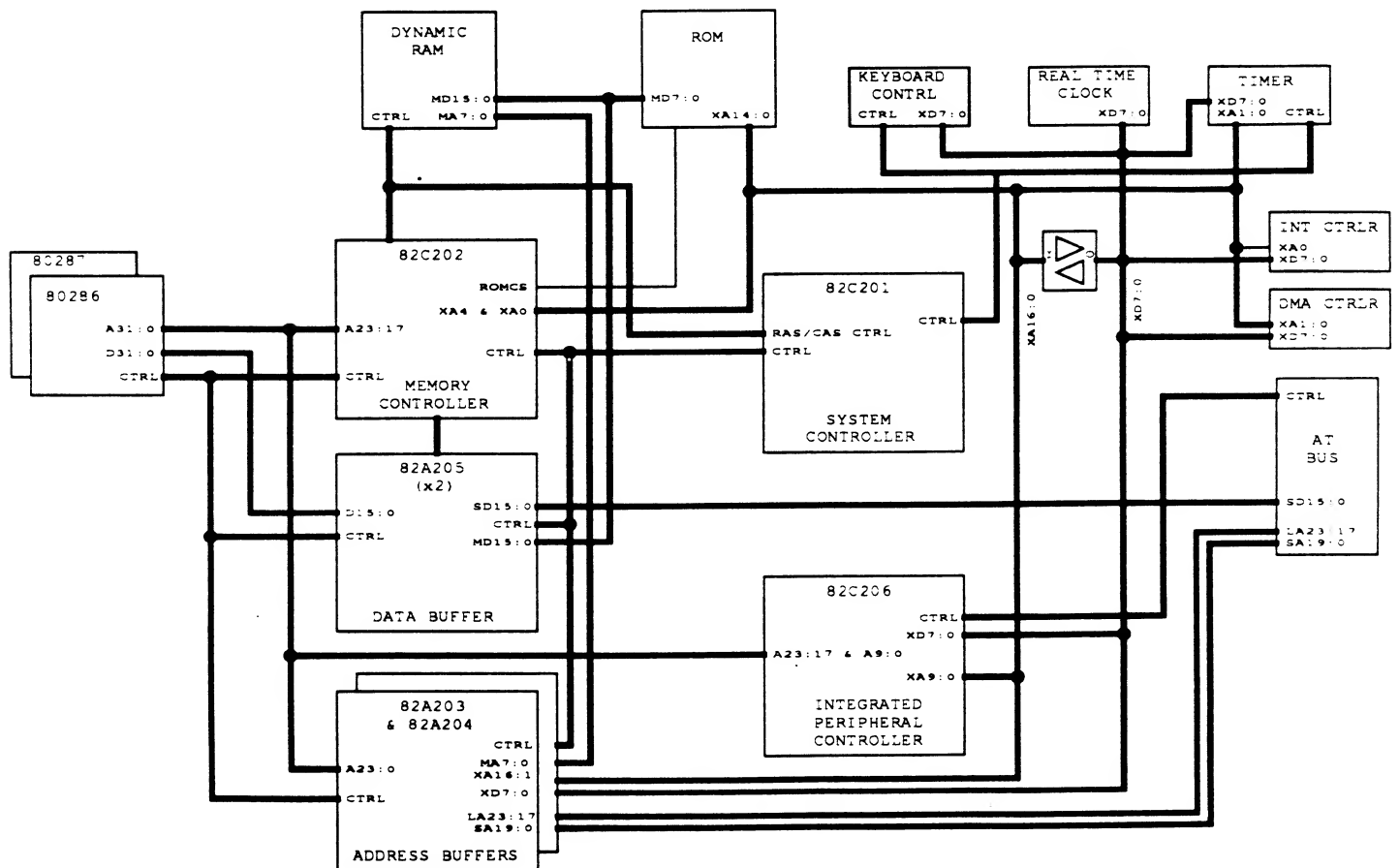
Provides low byte to high byte translation

Provides parity generation/checking logic

**Cache:** No

**Clock Speed:** 8 or 10 MHz

**Main Memory:** No



CS8220 Chips & Tech PC/AT Compatible Chipset

**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80286, 80386  
**System Bus:** AT  
**Part:** 82C206, Integrated Peripheral Controller  
**Availability:** 1986

**Cache:** No  
**Clock Speed:** up to 10 MHz  
**Main Memory:** Yes

**Second Source:** none  
**Functions Contained:**

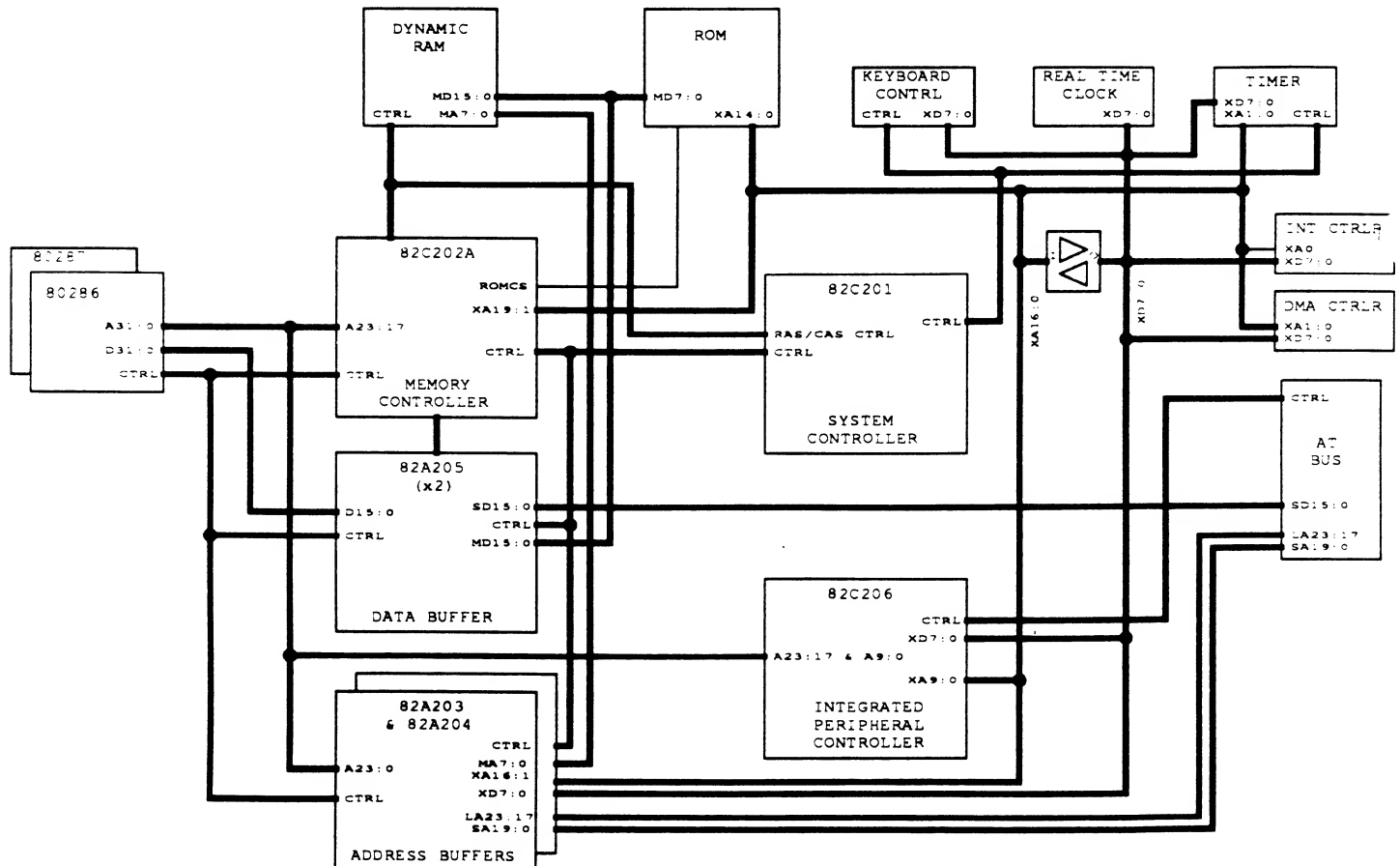
100% functionally compatible to IBM AT

- (1) 8284 compatible clock generator
- (2) 8237 compatible DMA controller (8 or 4 MHz)
- (1) 8254 compatible programmable timer/counter
- (1) 74LS612 compatible Memory Mapper

- (1) 8288 compatible bus controller
  - (2) 8259 compatible interrupt controller
  - (1) MC146818 compatible Real Time Clock
- Provides 114 bytes of CMOS RAM

Offers reduced recovery time (120ns) between control

Supports programmable wait state for DMA cycle



CS8220 Chips & Tech PC/AT Compatible Chipset



**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C211, CPU/Bus controller (part of CS8221 New Enhanced AT Data Book = NEAT)

**Availability:** 1988

**Second Source:** none

**Functions Contained:**

Clock generation with software speed selection

Optional independent AT bus clock

CPU and numeric processor interface and bus control

Programmable command delays and wait state generation

Provides reset and shut down logic

Provides DMA and refresh logic

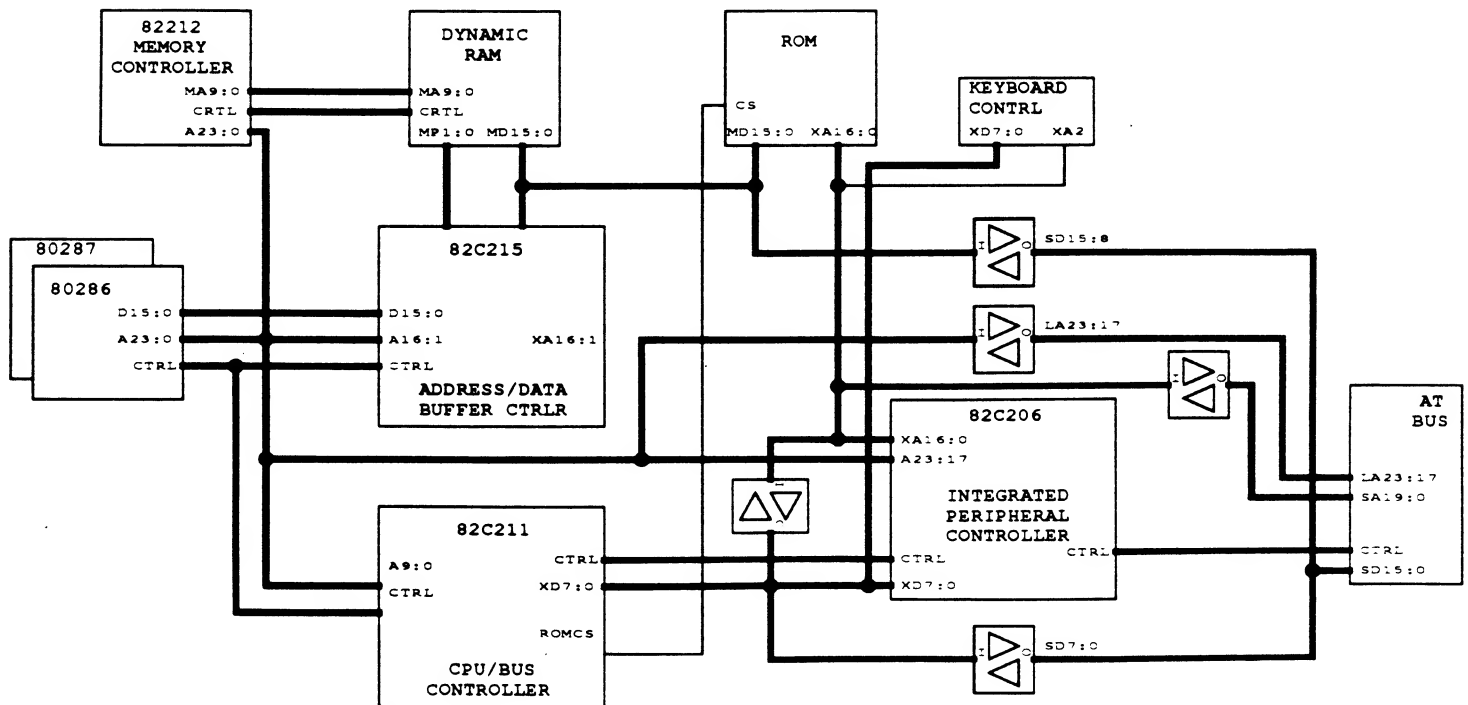
Provides action codes generation

Provides port B register and NMI logic

**Cache:** No

**Clock Speed:** 12 & 16 MHz

**Main Memory:** No



CS8221 New Enhanced AT Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C212, Page/Interleave and EMS Memory Controller (part of CS8221 New Enhanced AT Data Book = NEAT)

**Availability:** 1988

**Second Source:** none

**Functions Contained:**

Page mode access of 1-, 2-, 4-way page interleaved memory

Supports 100ns DRAMS at 16 MHz

Supports 256Kx1 or 1Mx1 DRAMS (in mixed mode)

Supports up to 8 MB on-board memory

Supports LIM EMS 4.0 address translation logic

Supports shadow RAM of BIOS

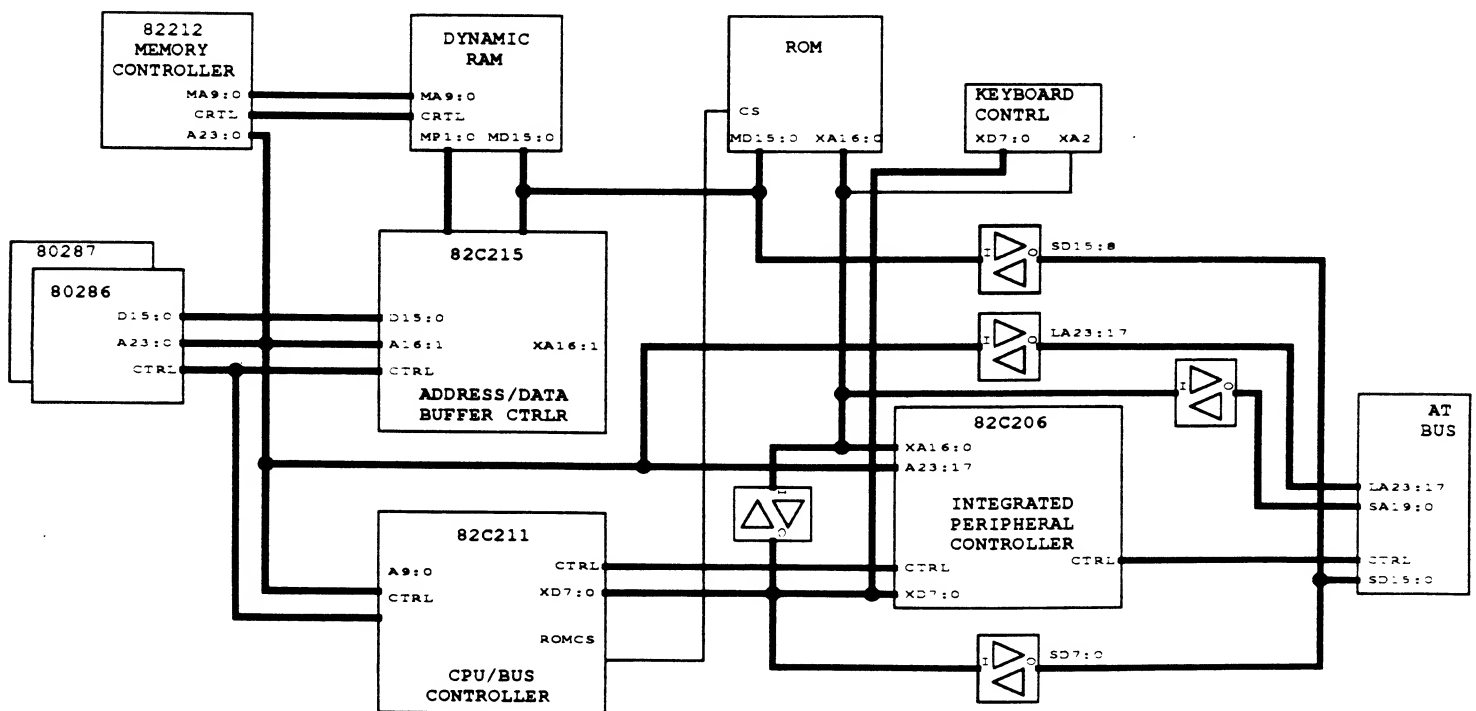
Supports fast switching between real & protected mode (OS/2)

Staggered refresh to reduce power supply noise

**Cache:** No

**Clock Speed:** 12 & 16 MHz

**Main Memory:** Yes



CS8221 New Enhanced AT Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C215, Data/Address Buffer (part of CS8221 New Enhanced AT Data Book = NEAT)

**Availability:** 1988

**Second Source:** none

**Functions Contained:**

Contains address buffers and latches

Contains data buffers and latches

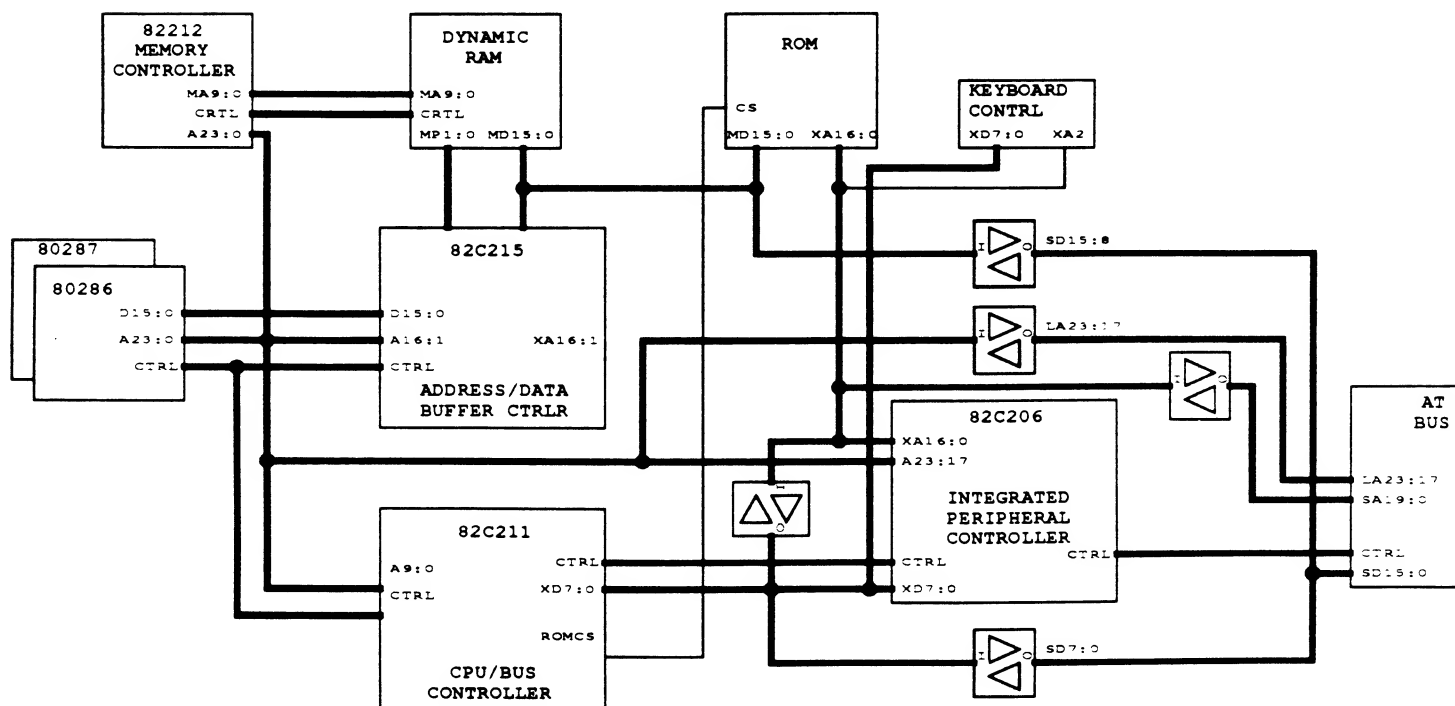
Provides bus conversion logic for 16-bit to 8-bit transfers

Provides parity generation/detection

**Cache:** No

**Clock Speed:** 12 & 16 MHz

**Main Memory:** No



CS8221 New Enhanced AT Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** MCA

**Part:** 82C221, MCA/CPU Controller (part of CHIPS/250 Model 50/60 Compatible CHIPSet)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Programmable wait state option

Bus conversion for 8-bit devices

Supports Matched memory cycle

GateA20 generation

Clock generation and selection logic

Supports master cycles

MCA bus memory and I/O cycles for 8, 16, 32 bit peripherals

**Cache:** No

**Clock Speed:** 10, 12.5, 16, 20 MHz

**Main Memory:** No

Provides fast VGA cycle

Numeric co-processor interface

Reset generation

Provides reset and shut down logic

CPU/DMA State machine

Bus conversion cycles

Schematic Not Available At Press Time

**Manufacturer:** Chips & Technologies**Processor Supported:** 80286**System Bus:** MCA**Part:** 82C222, EMS Memory Controller (part of CHIPS/250 Model 50/60 Compatible CHIPSet)**Availability:** 1989**Second Source:** none**Functions Contained:**

Page Mode access (single, 2-way, 4-way interleaved memory banks)

Supports remapping of RAM resident (640K-1MB) to top of 1MB

Supports 256Kx1, 256Kx4, 1Mx1, 1Mx4 DRAMs

Supports shadowing of BIOS into RAM

Supports page mode and Static Column DRAMs blocks)

Support for external EMS mapper chip

Provides EEPROM chip select logic

Provides asynchronous interface to DMA &amp; external bus masters

**Cache:** No**Clock Speed:** 10, 12.5, 16, 20 MHz**Main Memory:** No

Supports up to 8 MB of memory

Supports LIM EMS 4.0 address translation

Provides 16KB bad block remapping (up to 4 16K

Programmable wait state generation

Schematic Not Available At Press Time

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** MCA

**Part:** 82C223, DMA Controller (part of CHIPS/280 Model 70/80 Compatible CHIPSet)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Provides 8 independent DMA channels

8237 Register/program compatibility (in 1 mode)

16 MB memory addressing capability

Status signals compatible with 80286

Supports Read verification mode

Channels support either byte or word

Provides error recovery mechanism

Provides DRAM refresh logic support (256KB, 1MB & 4MB DRAMs)

Contains Central Arbitration Control Point (CACP) - 16 levels

**Cache:** No

**Clock Speed:** 16, 20, 25 & 33 MHz

**Main Memory:** No

Supports Extended mode operation

64K I/O addressing capability

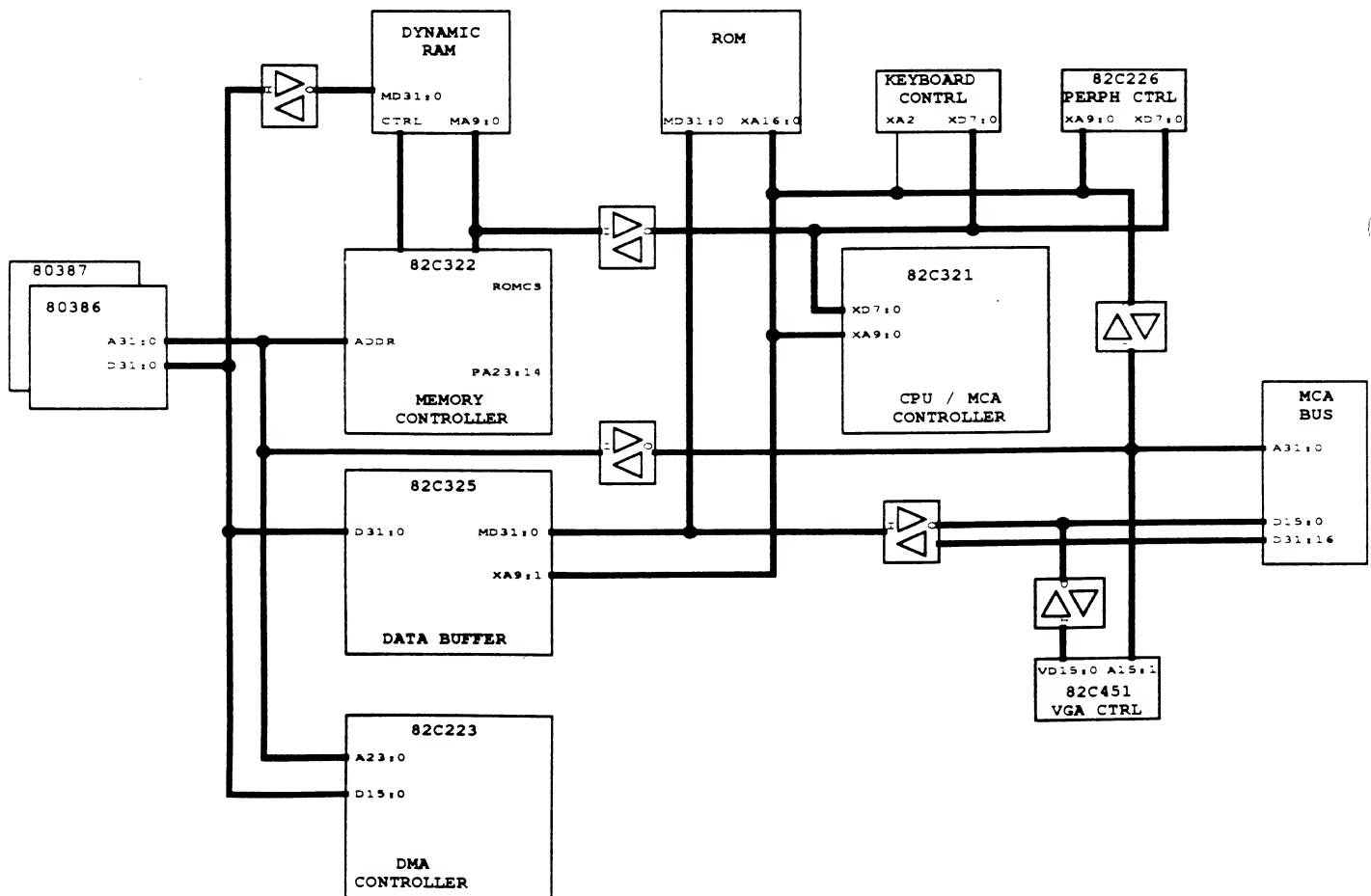
Data transfer between memory & I/O

Supports Serial DMA operation

Virtual DMA support for channels 0 & 4

NMI bus time out capability

Provides Refresh clock generation



**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** MCA

**Part:** 82C225, Data Buffer (part of CHIPS/280 Model 70/80 Compatible CHIPSet)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Data buffer latch

Controls transactions between CPU (LD) and memory (MD) data buses

Bus conversion for 8-bit data transfers

Provides bus steering for DMA and 16-bit masters

Provides parity generation/detection logic

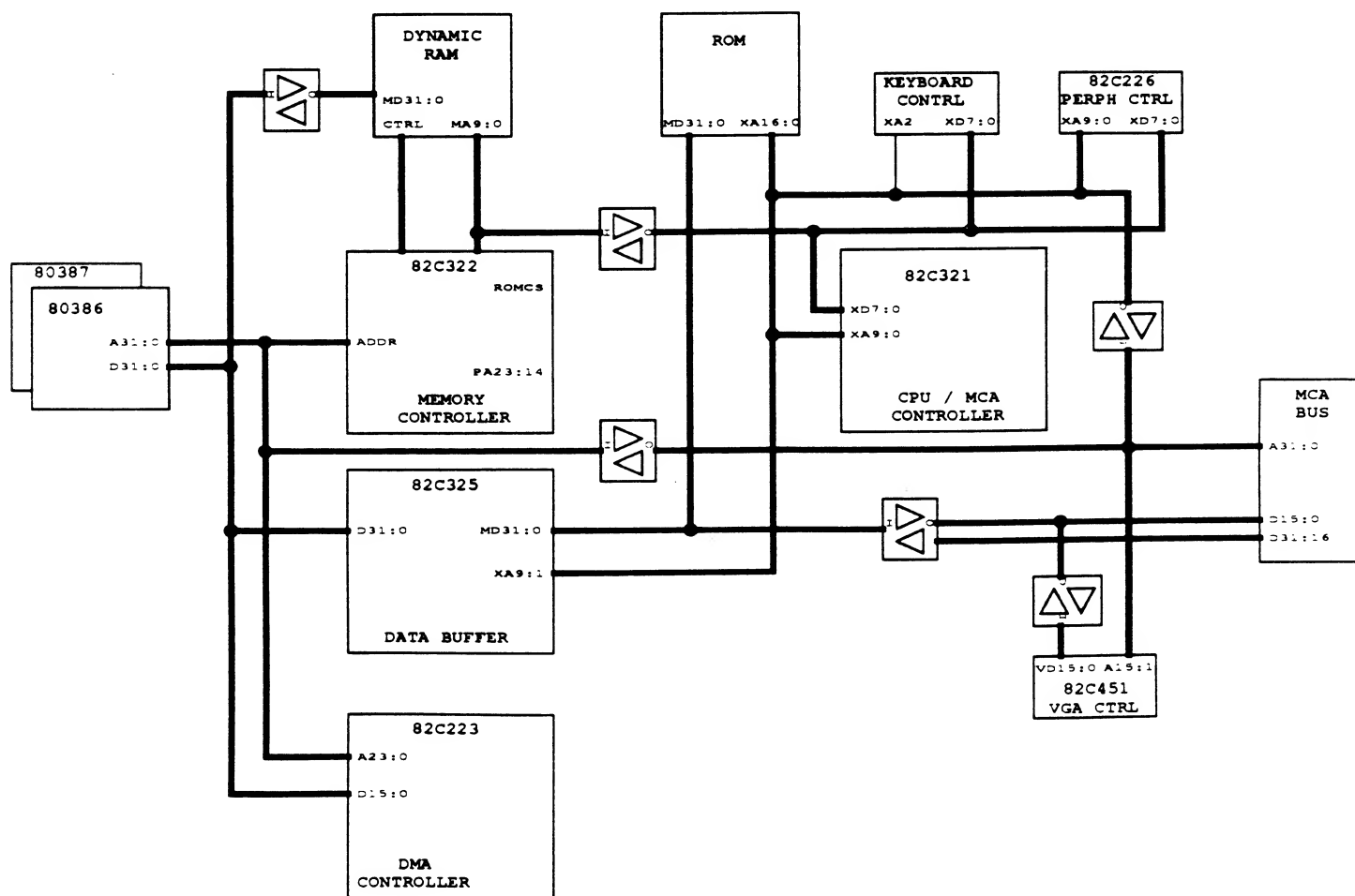
Universal programmable I/O ports & decoder

User programmable address decode registers and IBM PS/2 compatible POS registers

**Cache:** No

**Clock Speed:** 10, 12.5, 16, 20 MHz

**Main Memory:** No



**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** MCA

**Part:** 82C226, System Peripheral Controller (part of CHIPS/280 Model 70/80 Compatible CHIPSet)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

(2) 8259 compatible interrupt controller

(1) 146818 compatible Real Time Clock (RTC)

Provides 114 bytes of CMOS battery backed RAM

(3) System control registers

Programmable I/O decode signals (used in CHIPS250 system)

**Cache:** No

**Clock Speed:** 16, 20, 25 & 33 MHz

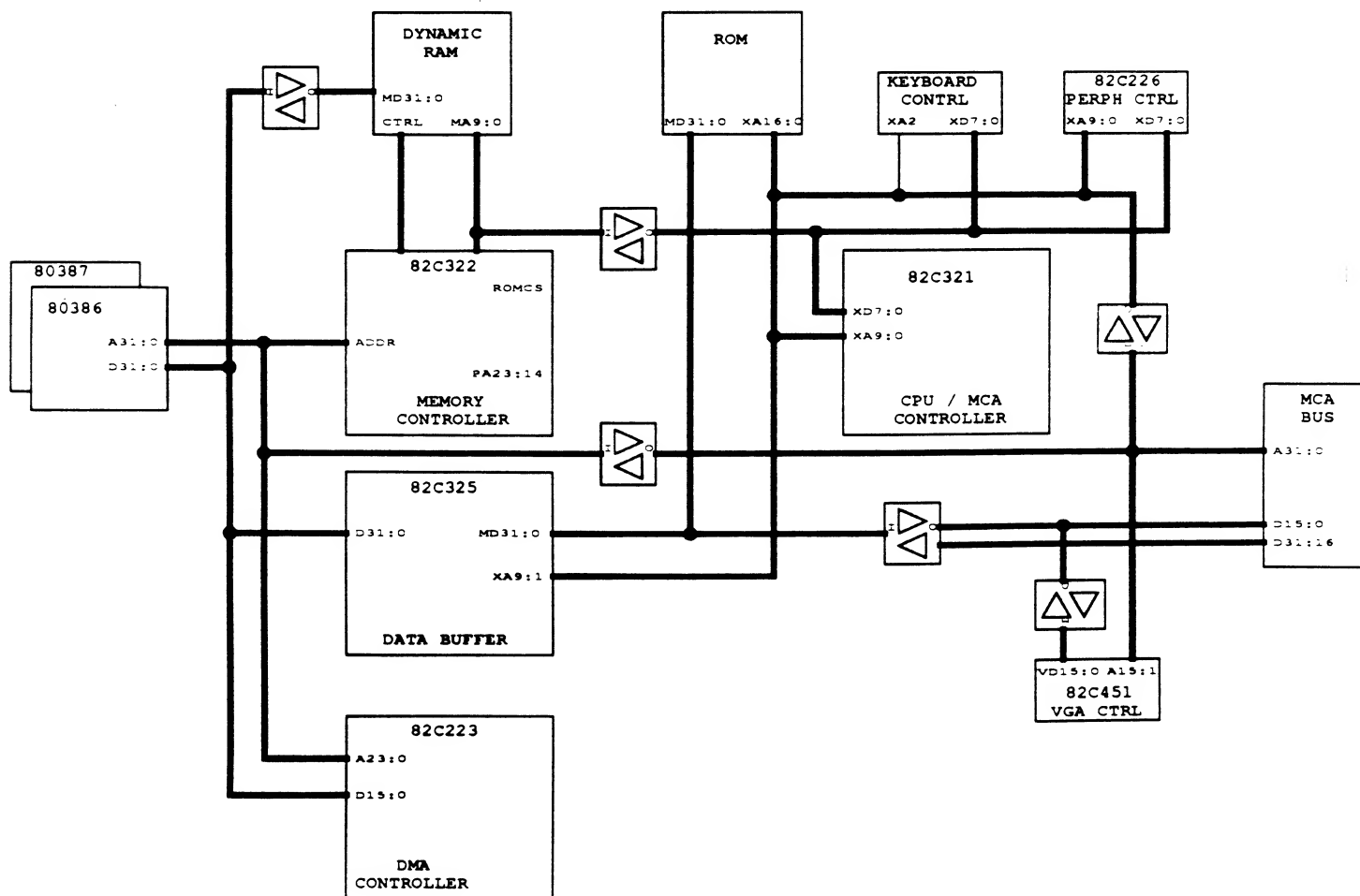
**Main Memory:** No

(1) 8254 compatible timer/counter

Watchdog timer

(1) 8-bit bi-directional parallel port

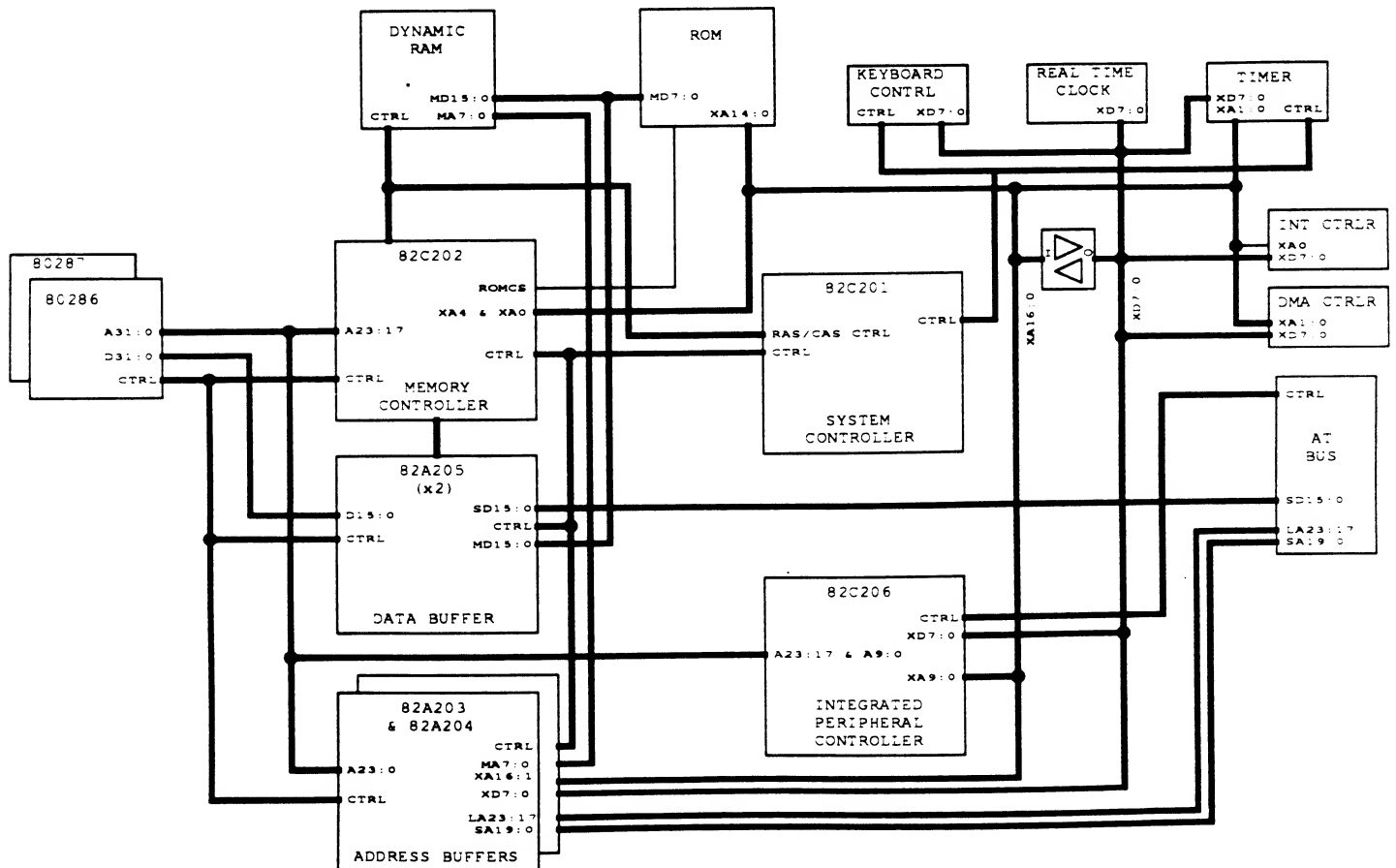
Provides card setup signals





**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80286  
**System Bus:** AT  
**Part:** 82C230, PS/2 Model 30 System Controller  
**Availability:** 1990  
**Second Source:** none  
**Functions Contained:**  
 Memory controller with onboard EMS  
 Bus interfaces & conversion logic  
 (1) 8237 compatible DMA controller  
 (1) 8259 compatible interrupt controllers  
 Peripheral chip-selects  
 Supports LIM EMS 4.0  
 Supports 64K x 1, 256K x 1, & 1M x 1 DRAMs  
 Programmable numeric processor frequency

**Cache:** No  
**Clock Speed:** 8, 10, 12.5 & 16 MHz  
**Main Memory:** Yes  
 Keyboard & mouse ports  
 Numerical Co-processor interface  
 (1) 8254 compatible programmable interval timer  
 (1) 8254 compatible interrupt controller  
 Supports up to 8 MB of memory  
 Supports shadow RAM  
 Programmable I/O channel timing for slower peripherals  
 Support for 8-bit or 16-bit BIOS ROMS



CS8220 Chips & Tech PC/AT Compatible Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C235, Single Chip AT

**Availability:** Q3 1989

**Second Source:** none

**Functions Contained:**

Provides control logic & clocks for 80286

(1) 146818 compatible Real Time Clock (RTC)

(2) 8237 compatible DMA controllers

(1) 8254 compatible programmable interval timer

(1) 82284 compatible clock generation

Supports shadow RAM (8-bit & 16-bit)

Supports LIM EMS 4.0 (32 EMS page registers)

Provides fast gate A20 and fast CPU reset logic

Supports up to 8 MB of DRAM (16 MB with 74F538 decoder)

**Cache:** No

**Clock Speed:** up to 12.5 MHz

**Main Memory:** Yes

114 bytes CMOS RAM

(2) 8259 compatible interrupt controllers

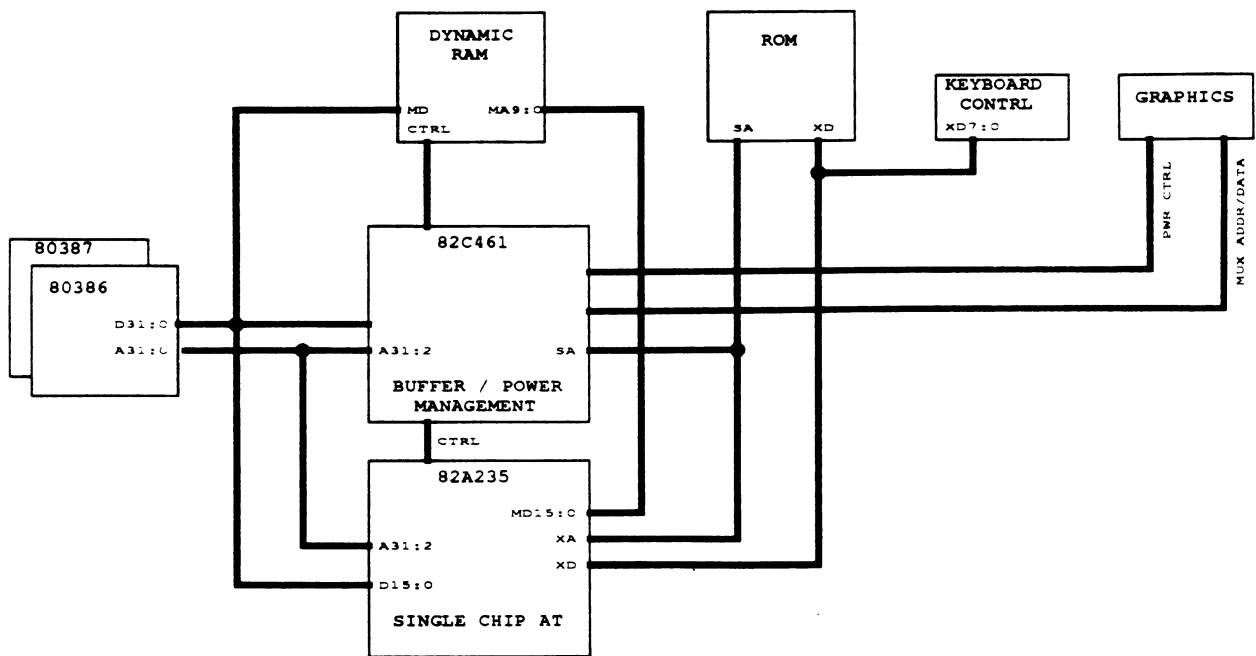
(1) 8255 compatible programmable peripheral interface

(1) 82288 compatible bus controller

Supports DRAM refresh

Provides 80287 and 8042 interface logic

Provides power management features



CHIPS11it• 82C461



## Personal Computer Design

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C242, Address/Data Buffers and Bus Controller (part of CS8223 LEAPset CHIPSet)

**Availability:** Q1 1990

**Second Source:** none

**Functions Contained:**

CPU and DMA address latches and buffers

CPU data buffers and latches

Bus conversion logic for 16-bit to 8-bit transfers

Parity generation/detection logic

Data buffers for local memory bus and local I/O bus

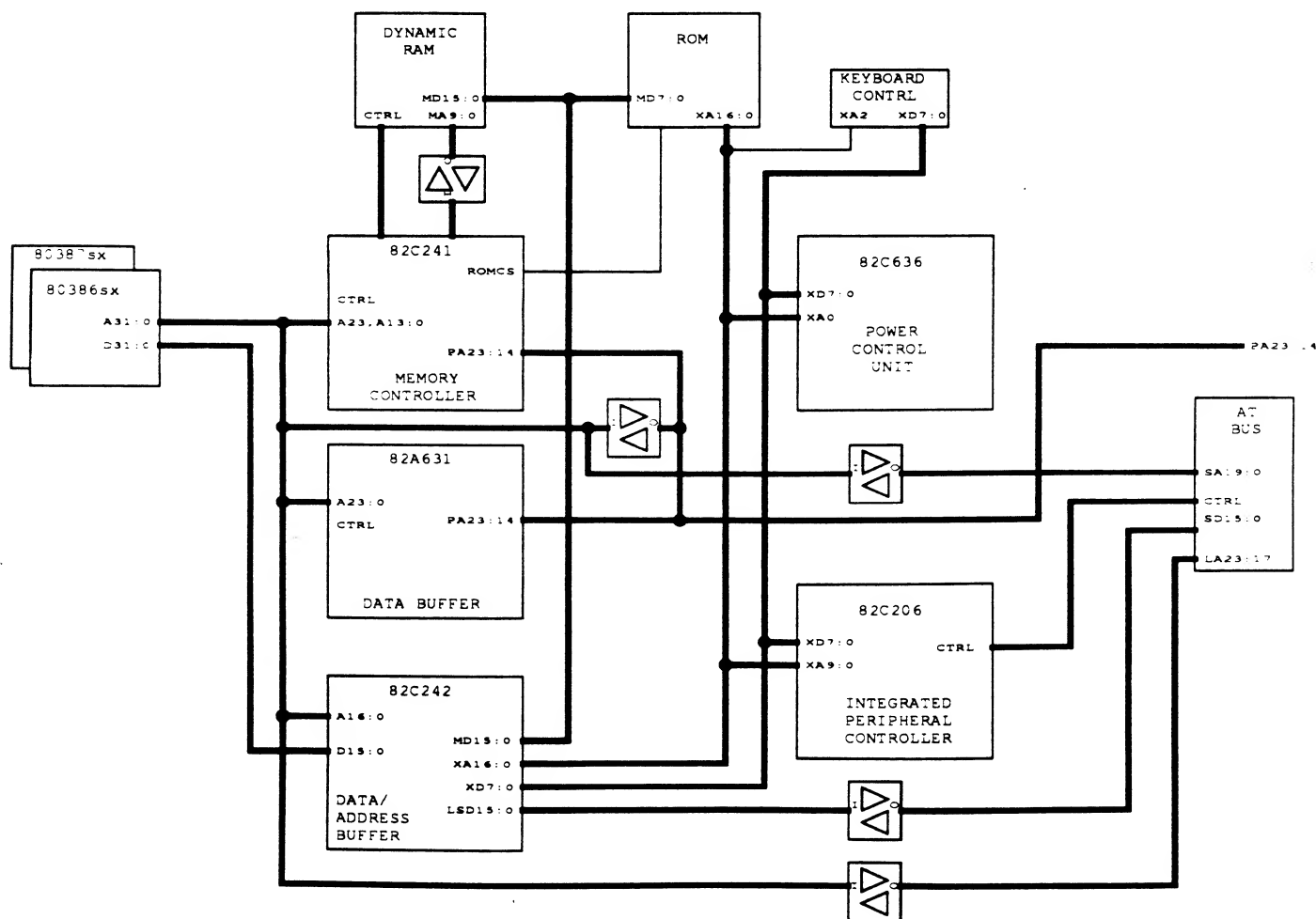
Data buffers for external AT bus

Oscillator circuit support of 14.31818 MHz crystal

**Cache:** No

**Clock Speed:** 12, 16 & 20 MHz

**Main Memory:** No



CS8223 Low-Powered AT Portable (LEAPsx) Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82C301, Bus Controller (part of CS8230:AT/386 CHIPSet)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Provides CPU interface and bus control

Interfaces directly with 80386

Provides processor clock selection

Provides AT bus access state machine

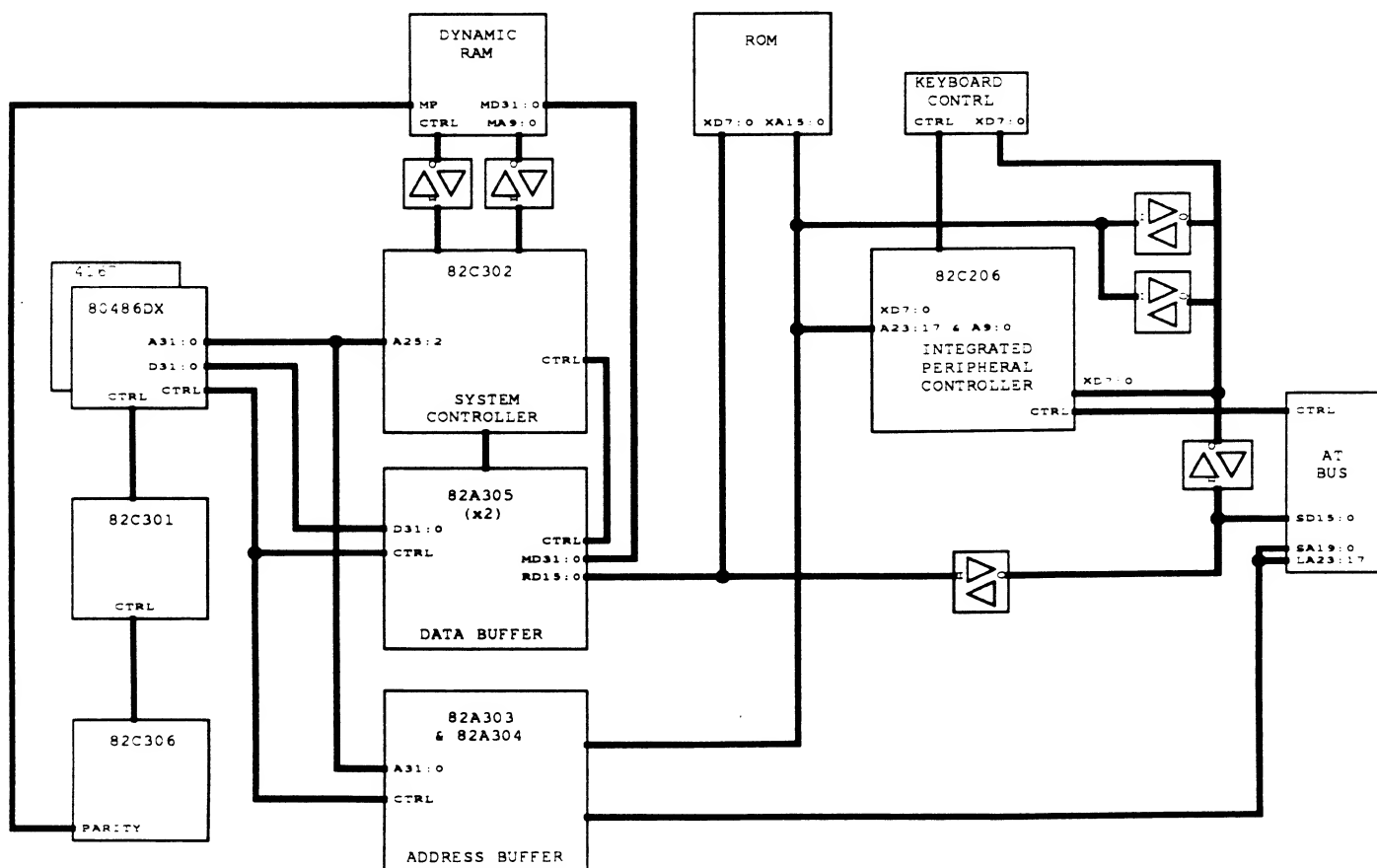
Provides port B register and NMI logics

Provides bus arbitration and refresh logic

**Cache:** No

**Clock Speed:** 16, 20, 25 MHz

**Main Memory:** No



CS8230 Chips & Tech AT386 Chipset

## Personal Computer Design

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82C302, Page/Interleave Memory Controller (part of CS8230:AT/386 CHIPSet)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Provides page mode access with interleaved memory banks (1,2 or 4 banks with 2KB pages)

Supports zero wait state access (100 ns DRAM)

Supports 256Kx1 and 1Mx1 DRAMs

Supports from 1MB to 16MB on-board memory

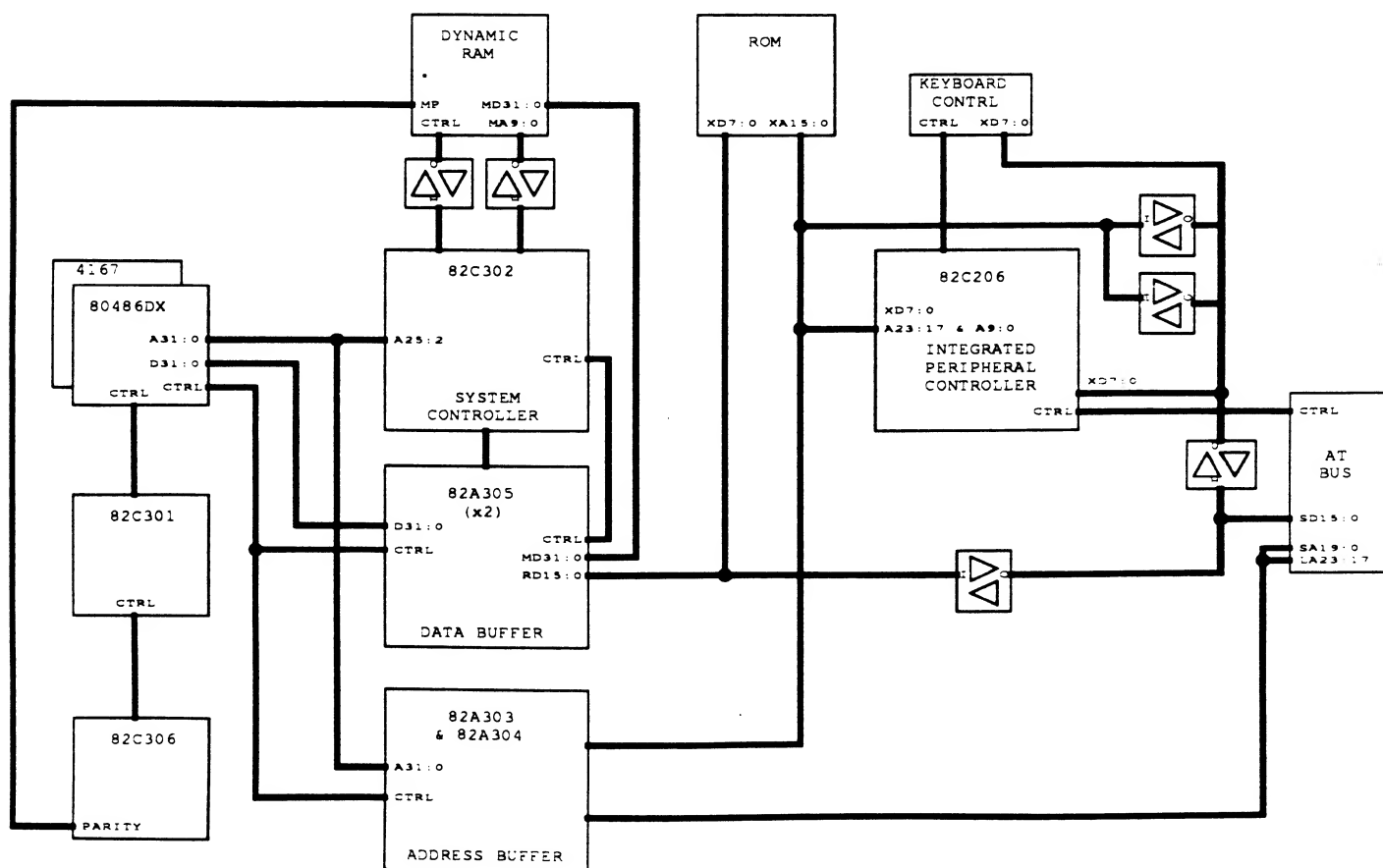
Supports from 1, 2 or 4 banks

Provides staggered refresh (cuts down power supply noise)

**Cache:** No

**Clock Speed:** 16, 20, 25 MHz

**Main Memory:** Yes



CS8230 Chips & Tech AT386 Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82A303/82C303, High Address Buffer (part of CS8230:AT/386 CHIPSet)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Provides a buffer for bits 31:12 of local, x, and system address buses

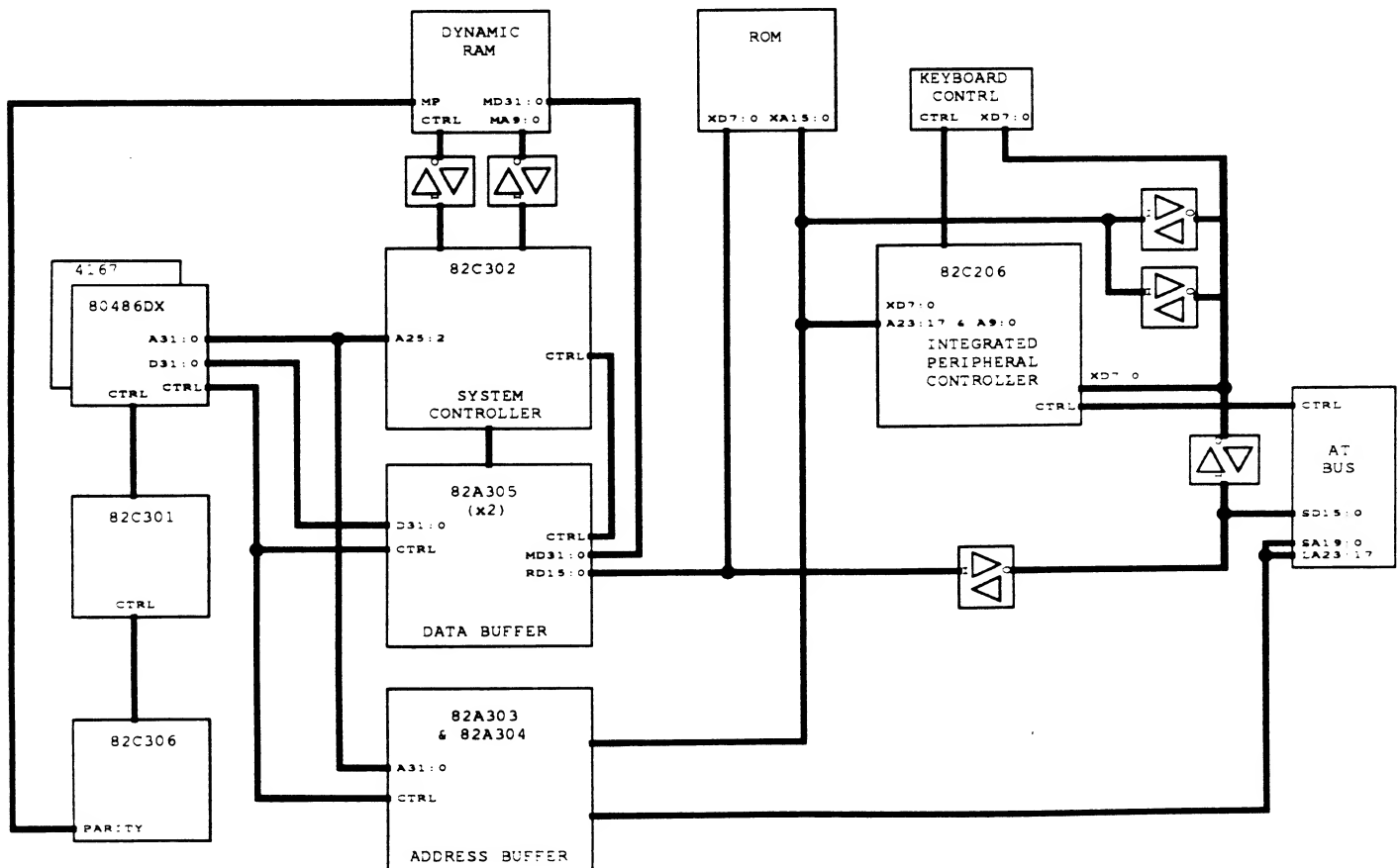
Allows for the extension of X and S address buses to 17-bits

Direct interface to AT bus

**Cache:** No

**Clock Speed:** 16, 20, 25 MHz

**Main Memory:** No



CS8230 Chips & Tech AT386 Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82A304/82C304, Low Address Buffer (part of CS8230:AT/386 CHIPSet)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Provides a buffer for bits 11:0 of local, x, and system address buses

Provides peripheral device decode

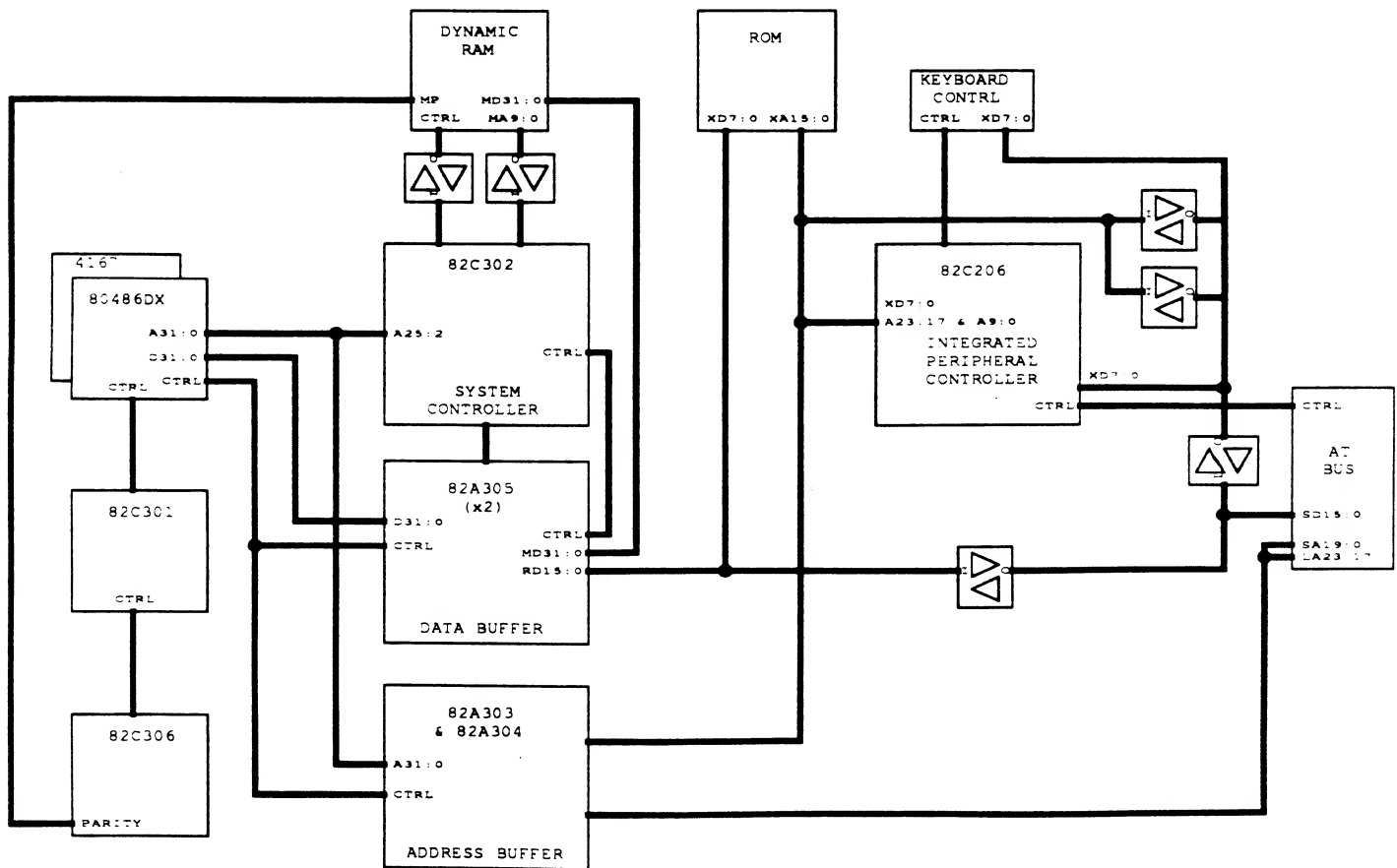
Direct interface to AT bus

Provides refresh address generation

**Cache:** No

**Clock Speed:** 16, 20, 25 MHz

**Main Memory:** No



CS8230 Chips & Tech AT386 Chipset



**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82A305/82B305/82C305, Data Buffer (part of CS8230:AT/386 CHIPSet)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Interfaces between local, memory and system (AT IO channel) data buses

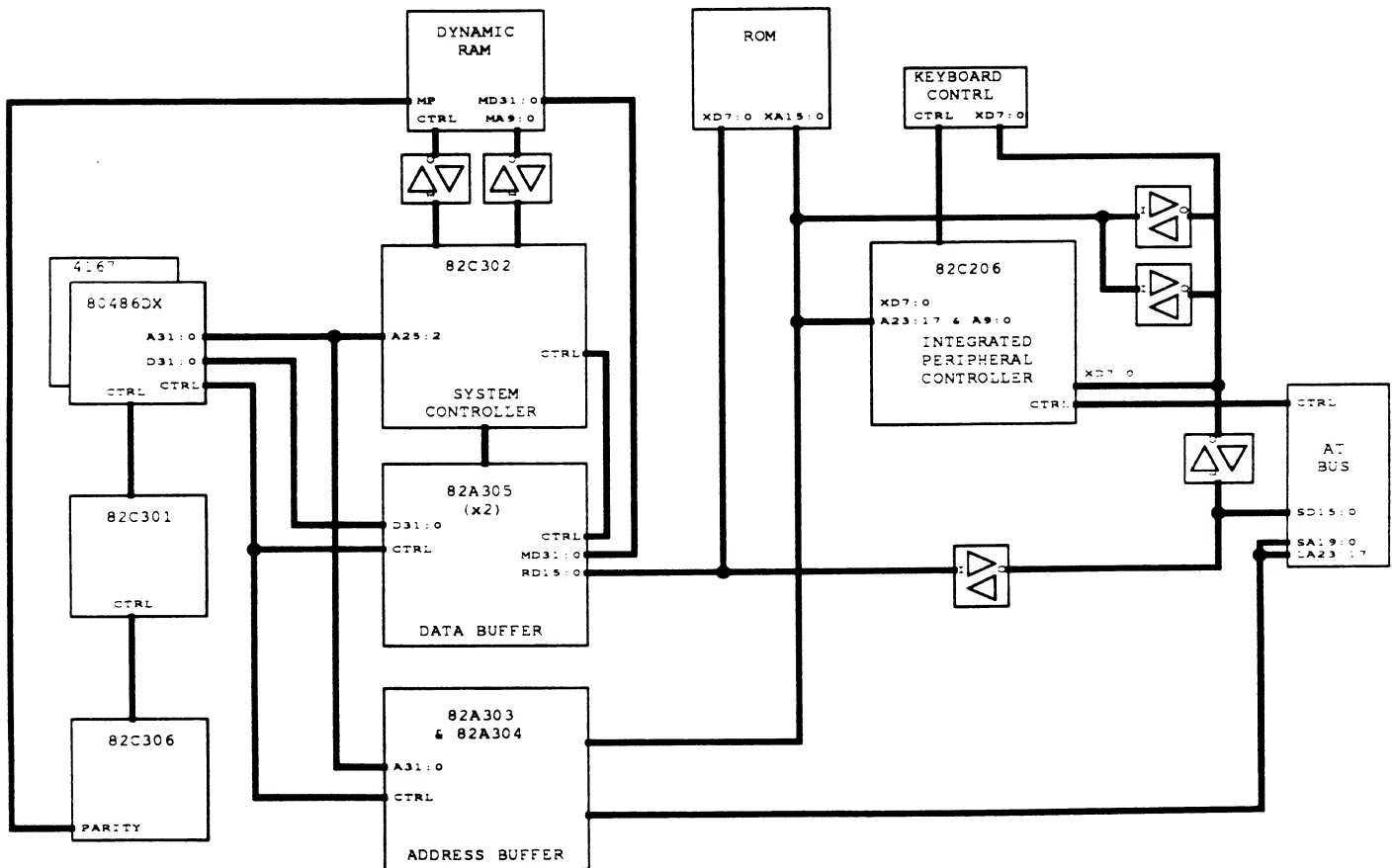
Provides data alignment and size conversion (32- or 16-bit to 32/16/8-bit)

Designed as nibble slice

**Cache:** No

**Clock Speed:** 16, 20, 25 MHz

**Main Memory:** No



CS8230 Chips & Tech AT386 Chipset

## Personal Computer Design

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82A306/82C306, Control Buffer (part of CS8230:AT/386 CHIPSet)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Provides 14.318 MHz oscillator and divide by 12 counter

Provides byte enable latch

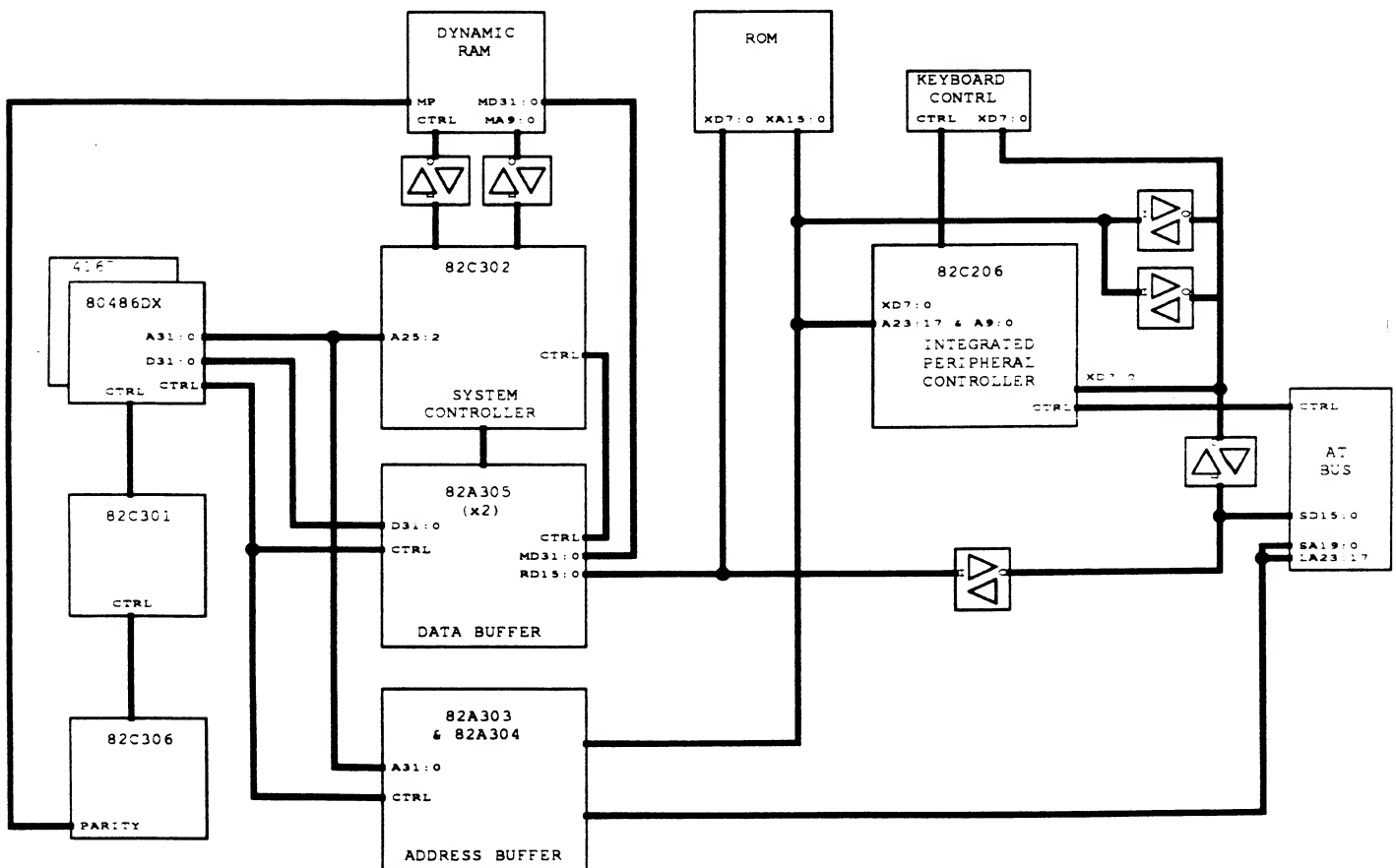
Provides parity generation/checking (with 82A305)

Contains direct interface to AT bus

**Cache:** No

**Clock Speed:** 16, 20, 25 MHz

**Main Memory:** No



CS8230 Chips & Tech AT386 Chipset

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82C307, Integrated Cache/DRAM Controller (part of CS8231:Turbo Cache-Based 386/AT CHIPSet)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Supports simultaneous activation of cache & DRAM access (minimize miss penalty)

Supports external 16/32 KB SRAM cache ( 2-way set associative)

Supports 32 byte line size, 4 byte sub-line size

Supports buffered write-through DRAM update

Supports zero wait state pipelined/non-pipelined reads & writes

On-chip tag RAM directory (accessible through peripheral data bus)

Supports 4 blocks of 4 banks of DRAM (1 MB to 64 MB)

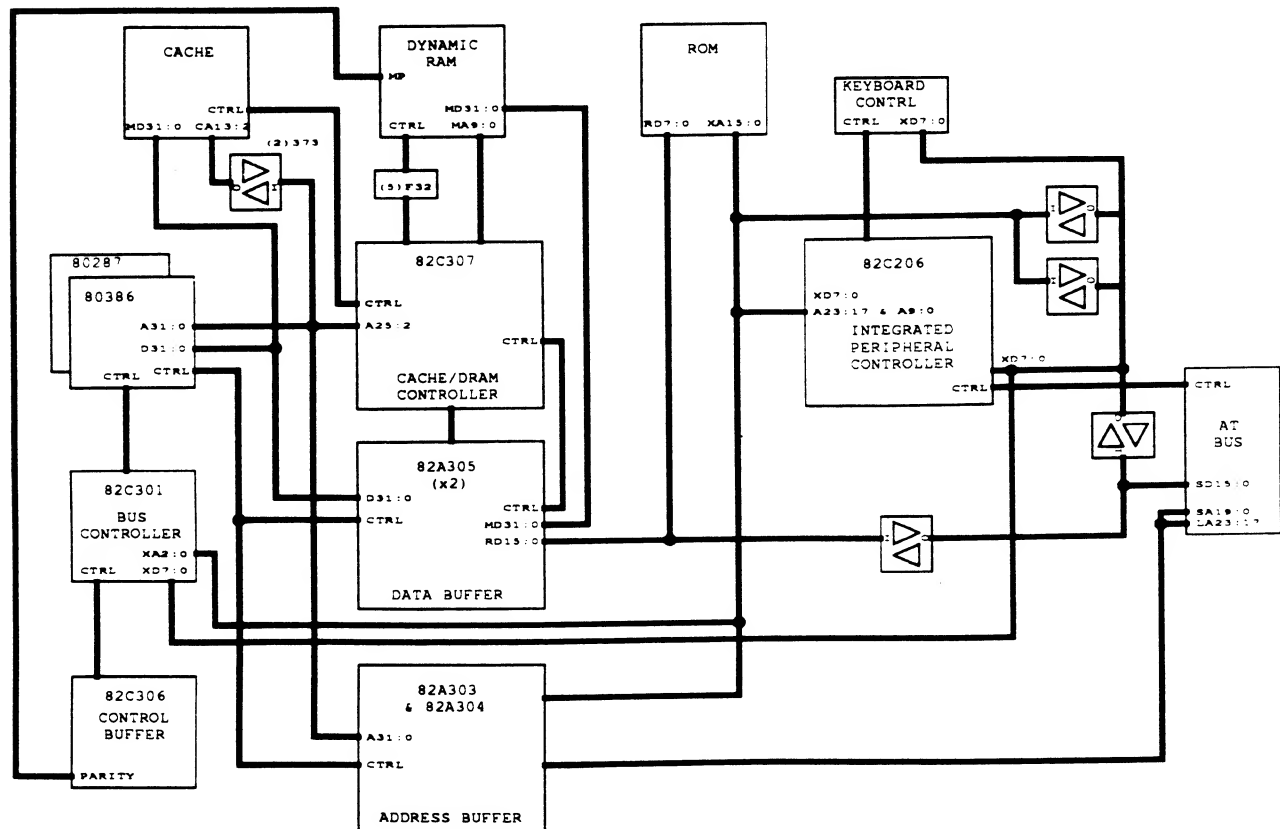
Supports 256Kx1, 256Kx4, 1Mx1, 1Mx4 DRAMs (mixed mode)

Provides access and refresh signals to DRAM

Allows 4 defined block (2KB to 128KB per block)

Optional Error Detection & Correction (EDC) support logic

DMA cycles channeled through controller logic (data from main memory)



**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** MCA

**Part:** 82C321, CPU Controller (part of CHIPS/280 Model 70/80 Compatible CHIPSet)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

100% MCA specifications at all CPU speeds

Matched memory cycle support

Bus conversion for 16- and 8-bit devices

Reset generation

MCA bus memory and I/O cycles for 8, 16, 32 bit peripherals

MCA compatible status (S0, S1), Address Decode Latch (-ADL) and Command (-CMD) generation

**Cache:** No

**Clock Speed:** 16, 20, 25 & 33 MHz

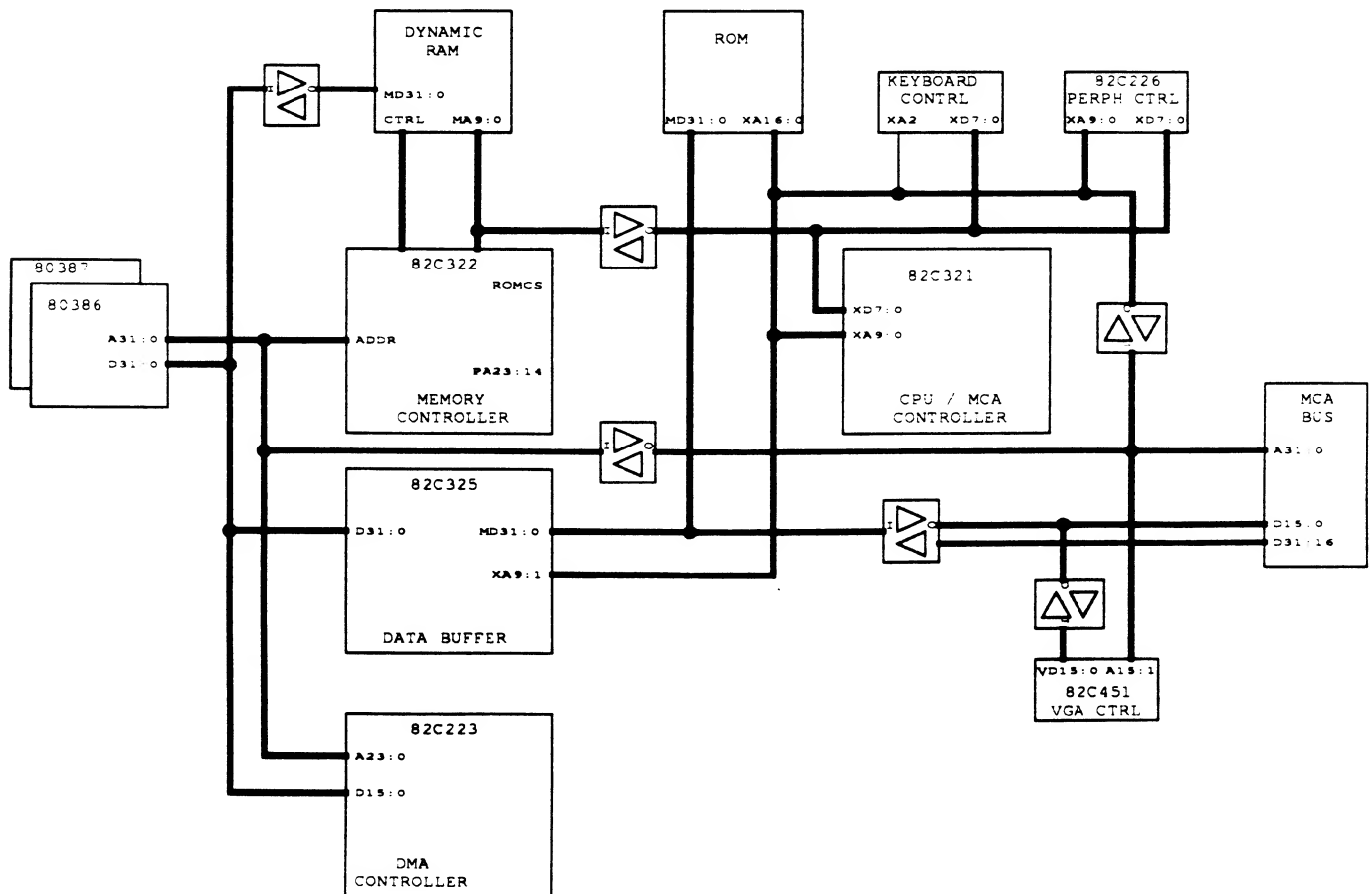
**Main Memory:** No

Programmable wait state option

Fast VGA cycle

80387 interface

GateA20 generation



CHIPS/280 Model 70/80 Compatible CHIPSet

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** MCA

**Part:** 82C322, Page/Interleaved Memory Controller (part of CHIPS/280 Model 70/80 Compatible CHIPSet)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Page Mode access (single, 2-way, 4-way interleaved memory banks)

Supports remapping of RAM resident (640K-896K or 512K-896K) to 1MB-15MB (on 1MB boundaries)

Supports 256Kx1, 256Kx4, 1Mx1, 1Mx4 DRAMs

Supports up to 16 MB of memory (4 banks)

Supports LIM EMS 3.2

Support for external EMS mapper chip

DRAMs locatable on CPU data bus

Provides 16KB bad block remapping (up to 4 16K blocks)

Supports staggered refresh to reduce power supply noise

Provides on-board I/O Logic and VGA decode logic

Compatible with PS/2 Model 80 Address Recovery logic

**Cache:** No

**Clock Speed:** 16, 20, 25 & 33 MHz

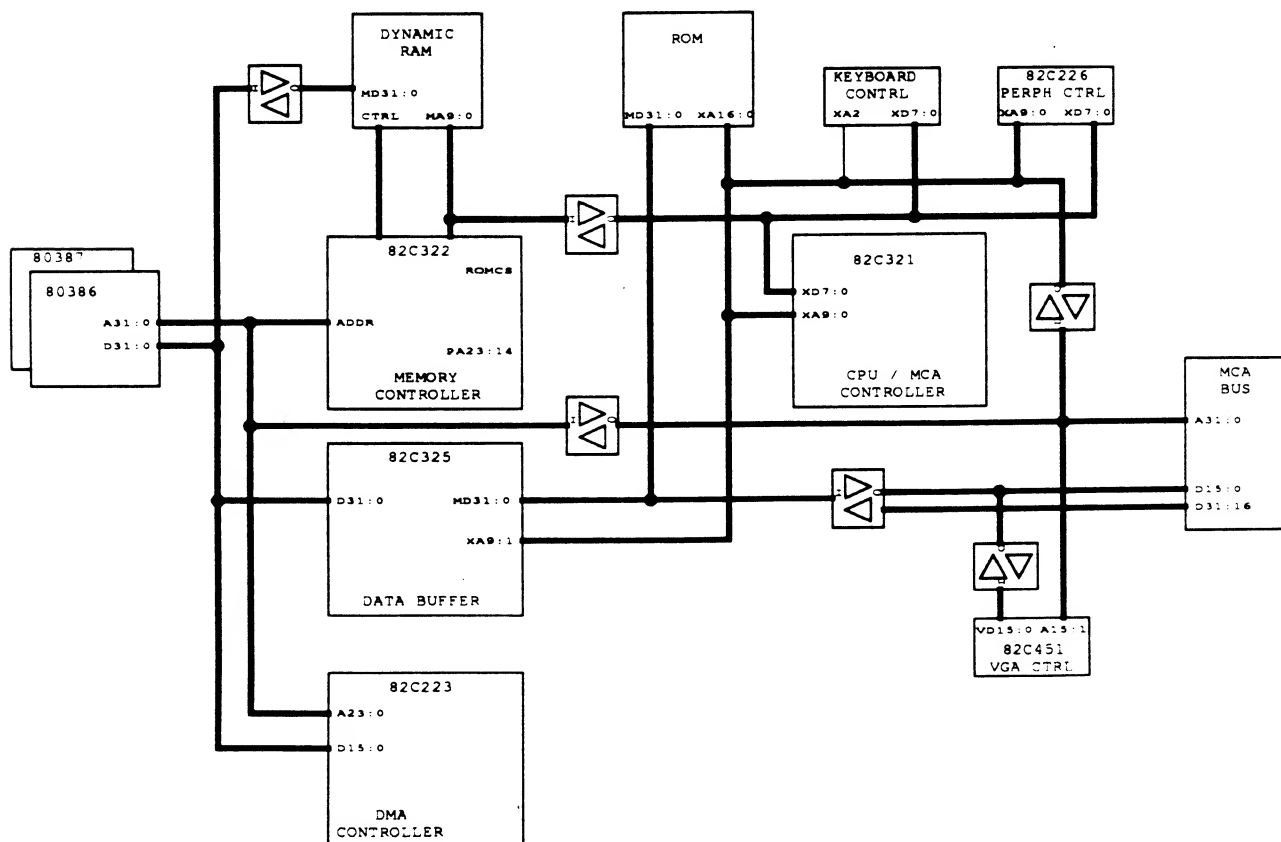
**Main Memory:** Yes

Supports shadowing of BIOS into RAM

Supports page mode DRAMs

Wait state generation

Provides EEPROM chip select logic



CHIPS/280 Model 70/80 Compatible CHIPSet

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** MCA

**Part:** 82C325, Data Buffer (part of CHIPS/280 Model 70/80 Compatible CHIPSet)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Data buffers and latches

Bus conversion for 32 bit to 16- or 8-bit data transfers

Provides bus steering for DMA and 16-bit masters

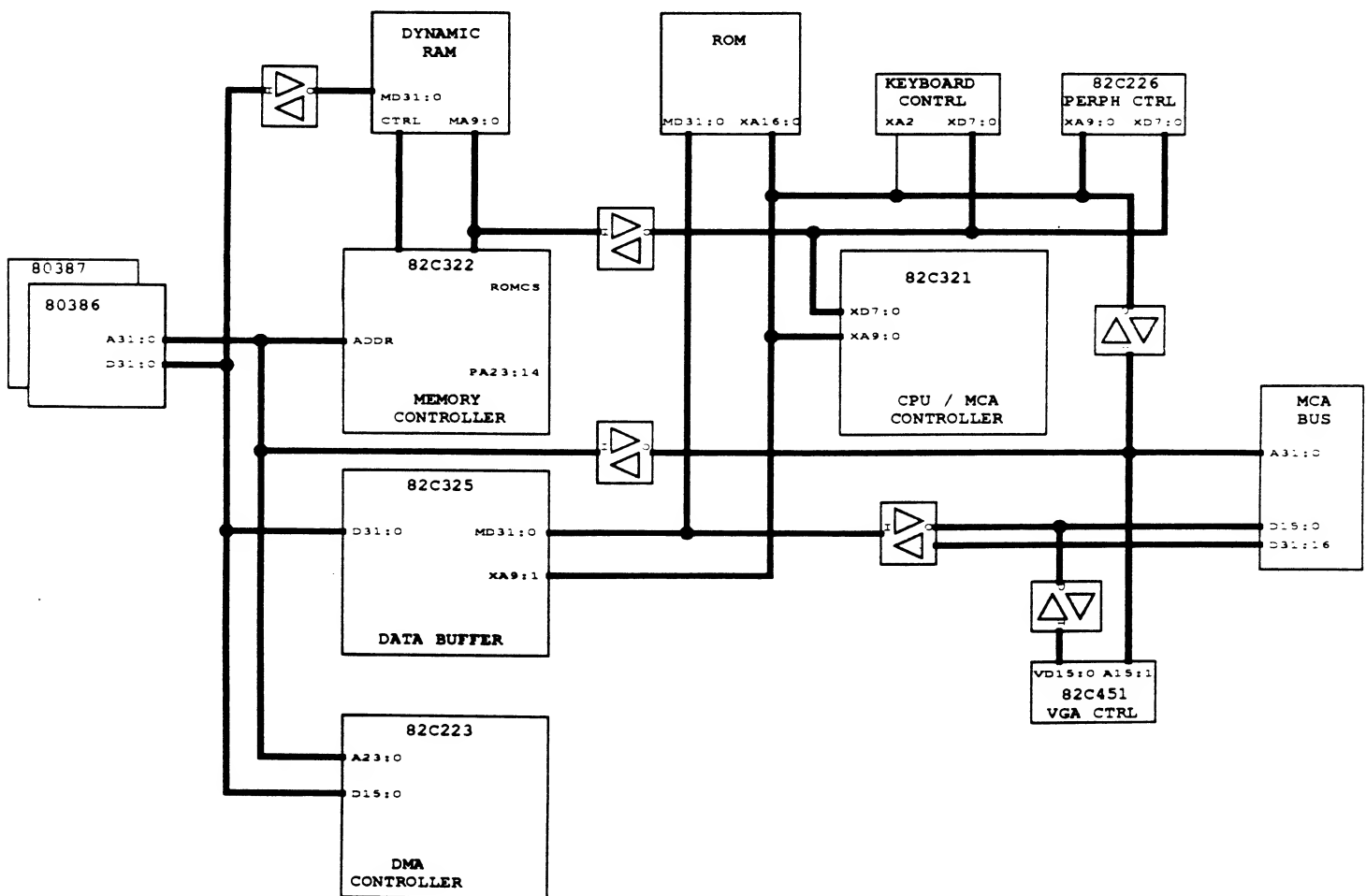
Provides parity generation/detection logic

User programmable address decode registers and IBM PS/2 compatible POS registers

**Cache:** No

**Clock Speed:** 16, 20, 25 & 33 MHz

**Main Memory:** No



**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** 82C351, CPU/Cache/DRAM Controller (part of CS82310 PEAK DM / 386 CHIPSet)

**Availability:** 1990

**Second Source:** none

**Functions Contained:**

State machines control CPU, DRAM, SRAM & AT bus cycles

Supports 32KB, 64Kb, 128Kb & 256KB direct mapped cache

Supports 128 MB main memory (DRAM)

Supports 256K, 1M, 4M DRAMs (up to 4 blocks of 2 banks)

Supports buffered write through

Supports DMA, refresh, shadow RAM & memory map

Supports (single) 512K or (double) 256K EPROMS

Supports port 92H fast reset and fast GATEA20

Programmable write 0 or 1 wait state 4, posted & non-posted

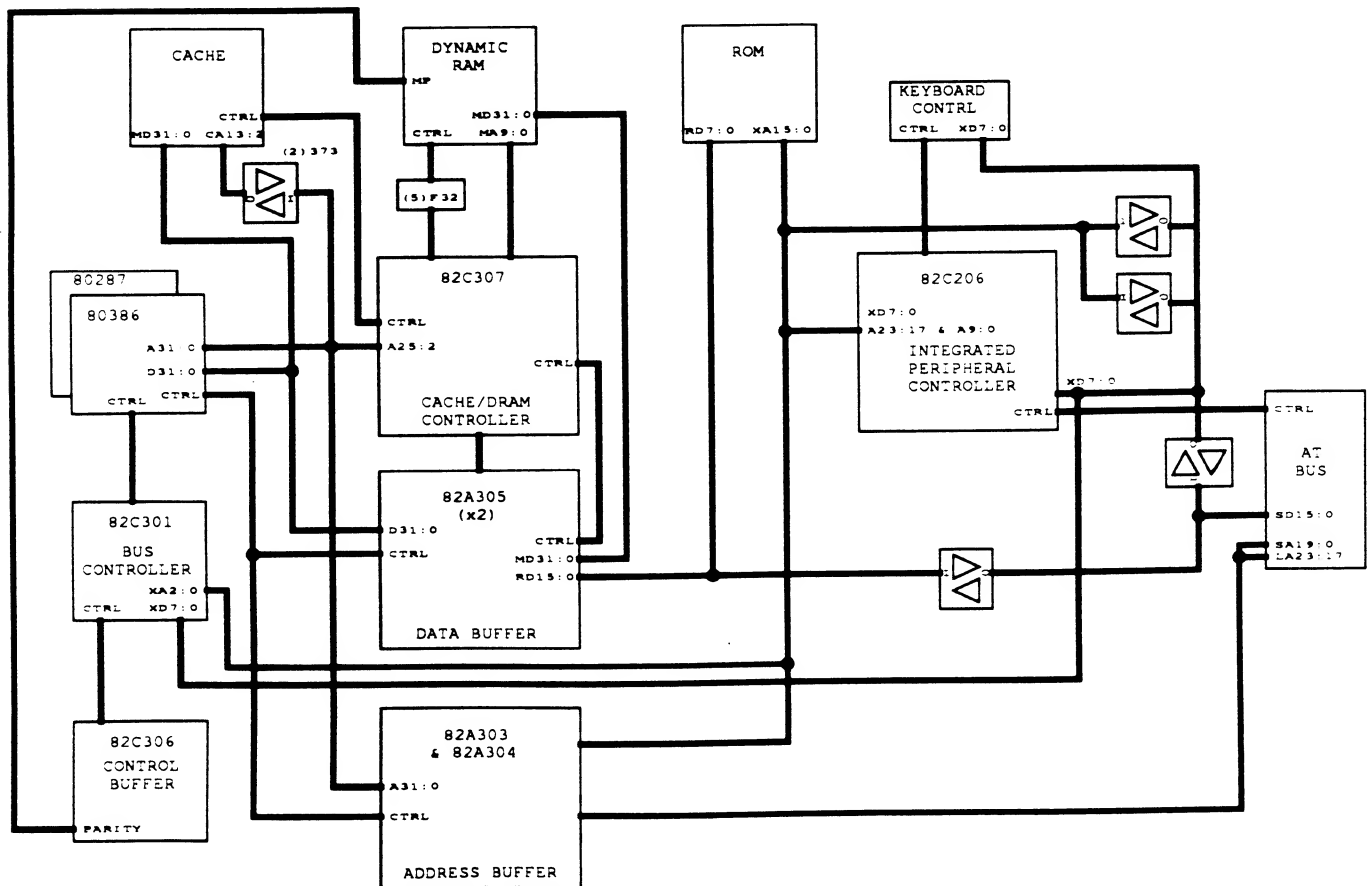
Supports non-cacheable regions

Integrated high speed tag cache comparator

**Cache:** Yes

**Clock Speed:** 25 & 33 MHz

**Main Memory:** Yes



CS8230 Chips & Technologies AT386 Chipset

## Personal Computer Design

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** 82C355, Data Buffer (part of CS82310 PEAK DM / 386 CHIPSet)

**Availability:** 1990

**Second Source:** none

**Functions Contained:**

Buffers data between D & MD buses

Provides parity generation/checking for DRAM

Latches data for DRAM buffered writes

Latches data from AT bus during CPU AT bus reads

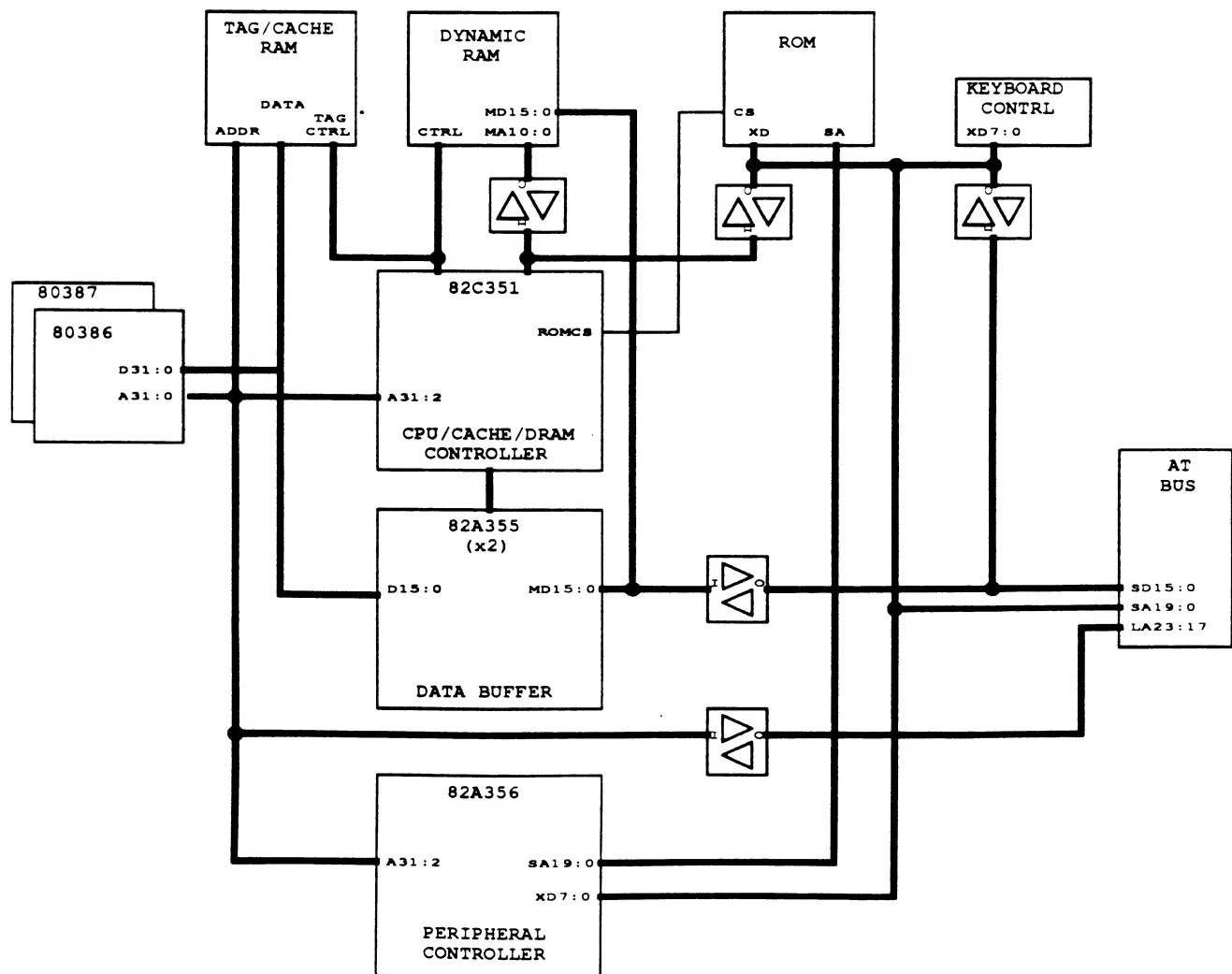
Performs data steering (data conversion) for AT bus accesses

Provides path for SD & XD buses

**Cache:** No

**Clock Speed:** 25 & 33 MHz

**Main Memory:** No





**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** 82C356, Peripheral Controller (part of CS82310 PEAK DM / 386 CHIPSet)

**Availability:** 1990

**Second Source:** none

**Functions Contained:**

(2) 8237 compatible DAM controllers

(1) 8254 compatible timer/counter

Real Time Clock (RTC)

Provides I/O address decodes

Provides port B and NMI logic

Provides address bus interface between A & SA buses

**Cache:** No

**Clock Speed:** 25 & 33 MHz

**Main Memory:** No

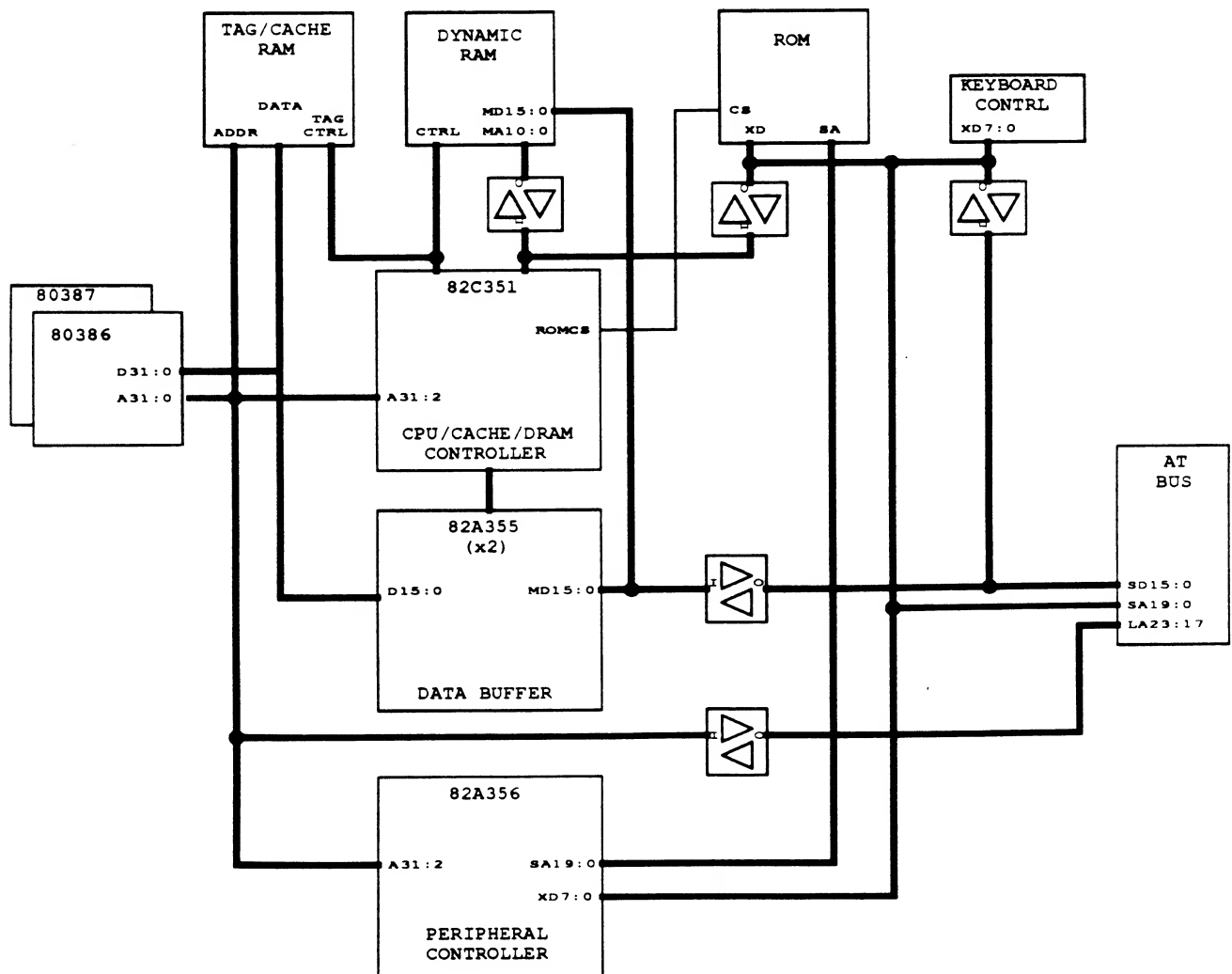
(2) 8259 compatible interrupt controllers

(1) 782LS612 memory mapper

CMOS memory

Contains 14.318 MHz oscillator interface

Configuration registers



**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT  
**Part:** 82C461, Buffer/Power Management Unit

**Cache:** No  
**Clock Speed:** ?  
**Main Memory:** No

**Availability:** not yet available

**Second Source:** none

### Functions Contained:

**Provides bi-directional address latches & buffers for 4 slot AT bus**

**Power Management handles transitions among power states (off, idle, stand-by, run)**

**Contains 2 power sense inputs and 2 user request inputs**

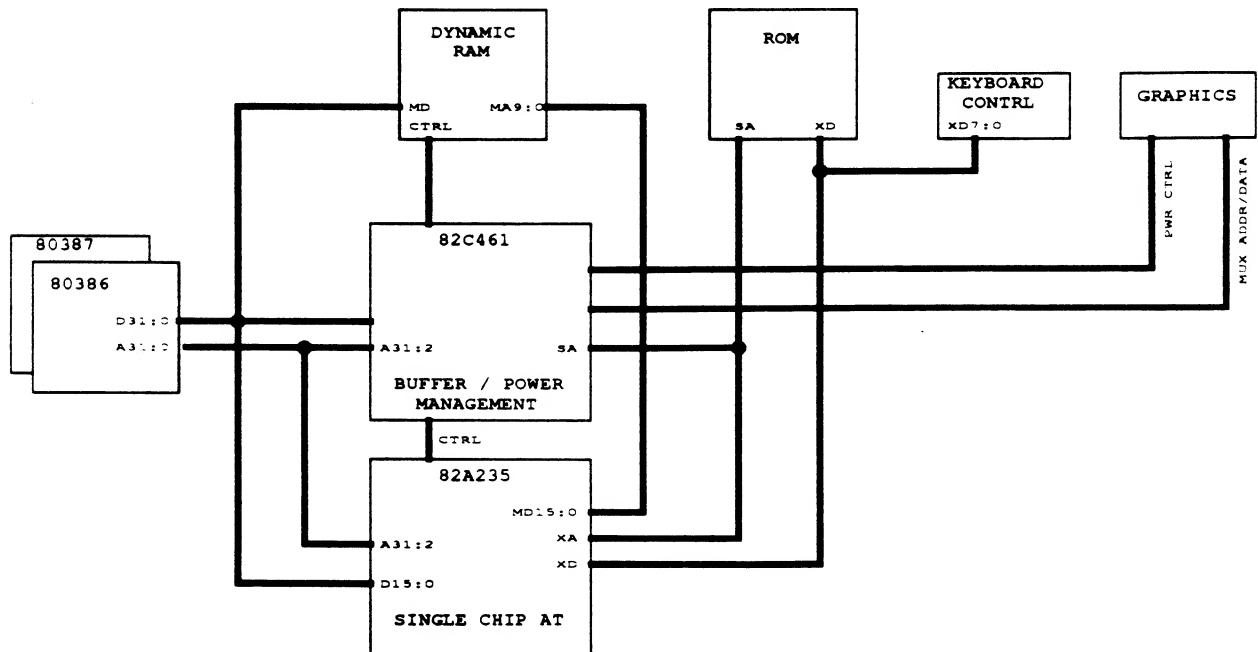
**Ring indicator counter and auto backlight power-off provided**

Provides 8 programmable I/O lines (PIO)

**Provides control lines for CHIPS graphics controllers**

**Provides buffers for data lines**

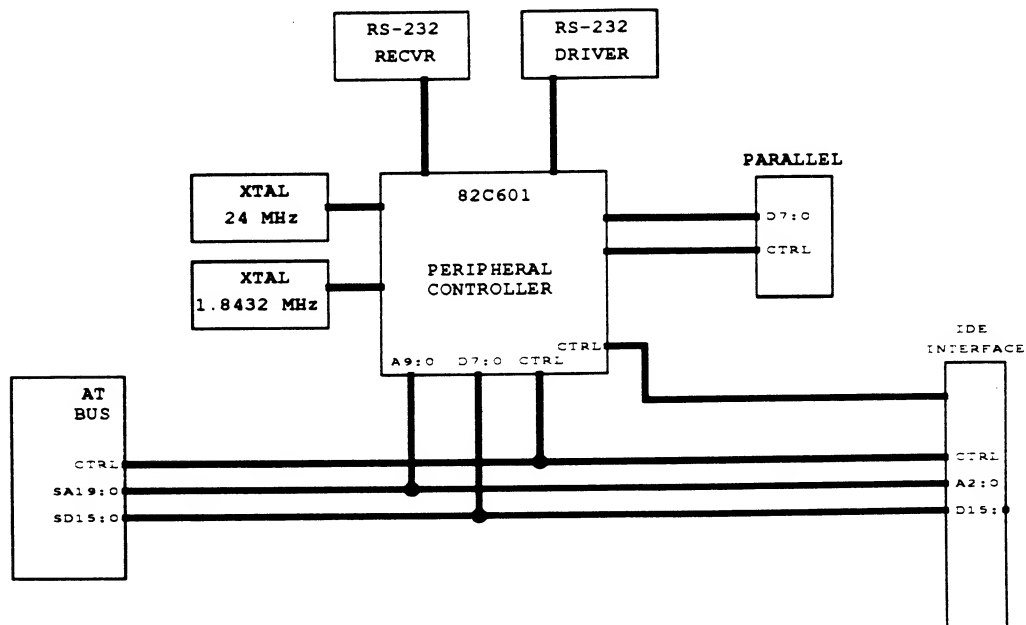
### NMI handler with 2 inputs



CHIPS1it 82C461

**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80286, 80386  
**System Bus:** XT/AT  
**Part:** 82C601, Single Chip Peripheral Controller  
**Availability:** 1989  
**Second Source:** none  
**Functions Contained:**  
 (2) 16450 compatible UARTS  
 Provides game port decode  
 Real Time Clock chip select  
 Provides 16 mA output drives  
 EISA ready (relocatable ports & IRQ, interrupt sharing)

**Cache:** No  
**Clock Speed:** ?  
**Main Memory:** No  
 (1) IBM XT/AT compatible Parallel port  
 Provides IDE interface  
 Power management features & power down modes  
 Provides internal address decoders



82C601 Single Chip Peripheral Controller

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C605, CHIPSpak/CHIPSport Multifunction Controllers

**Availability:** 1987

**Second Source:** none

**Functions Contained:**

Fully compatible with NS16450 asynchronous communications element

Provides parallel interface (printer or scanner)

Provides (2) UART channels - can be externally powered

Supports game port

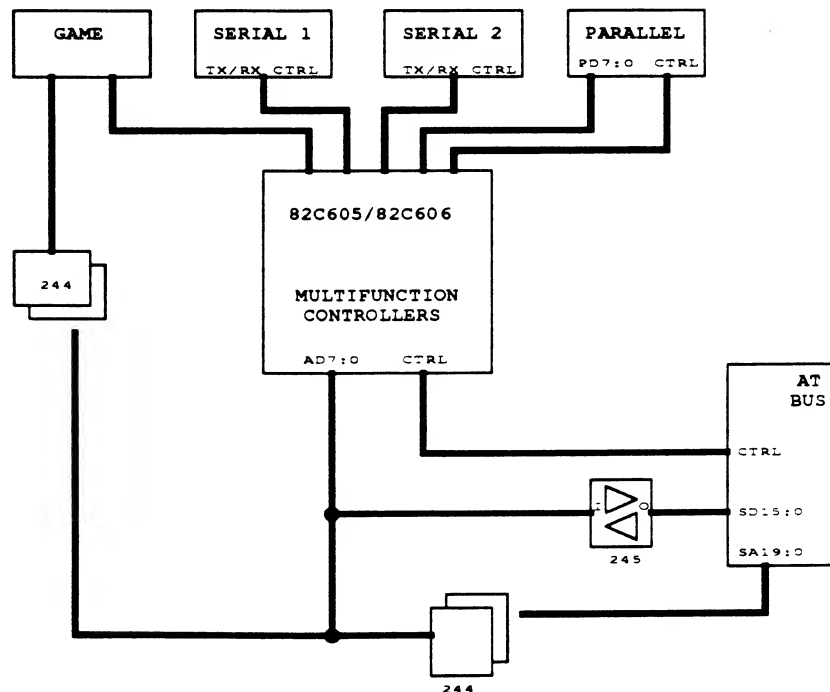
Provides 114 bytes of CMOS RAM

---

**Cache:** No

**Clock Speed:** ? MHz

**Main Memory:** No



Chips & Technologies 82C605/606 - CHIPSpak/CHIPSport Multifunction Controllers

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C606, CHIPSpak/CHIPSport Multifunction Controllers

**Availability:** 1987

**Second Source:** none

**Functions Contained:**

Provides parallel interface (printer or scanner)

Provides (2) UART channels - can be externally powered

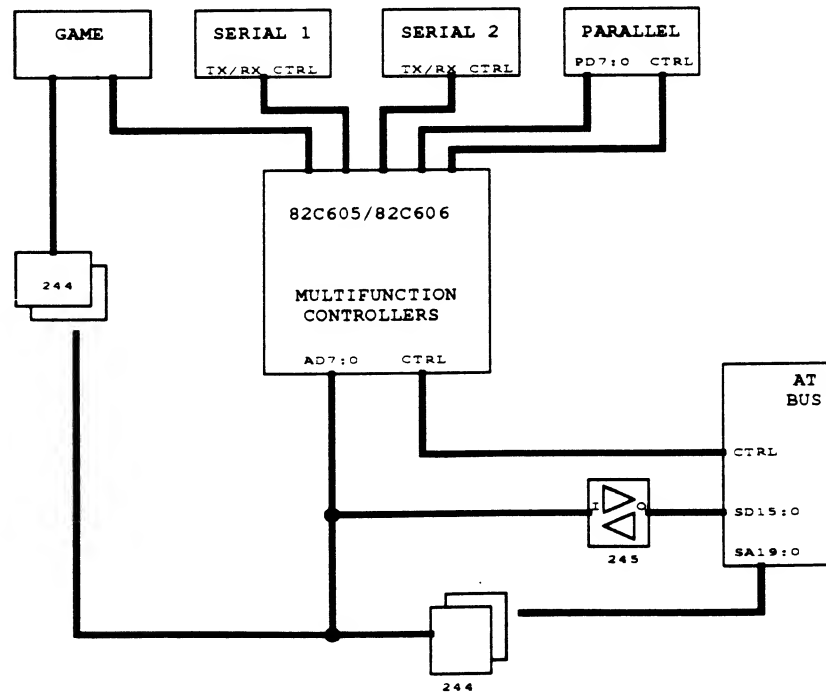
Fully compatible with NS16450 asynchronous communications element

Compatible with Motorola 146818A Real Time Clock (100 yr calendar)

CMOS configuration RAM (with battery backup) provides software selection of internal register base address

Supports game port

Provides 114 bytes of CMOS RAM



Chips & Technologies 82C605/606 - CHIPSpak/CHIPSport Multifunction Controllers

**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80286, 80386  
**System Bus:** AT  
**Part:** 82C607, Multifunction Controller

**Cache:** No  
**Clock Speed:** 24 MHz (XTAL)  
**Main Memory:** No

**Availability:** 1988

**Second Source:** none

**Functions Contained:**

100% functionally compatible to the IBM PS/2 model 50/60/80

UART is 100% compatible with NS16550 Asynchronous Communications Element

16 bytes FIFO transmit/receive buffers

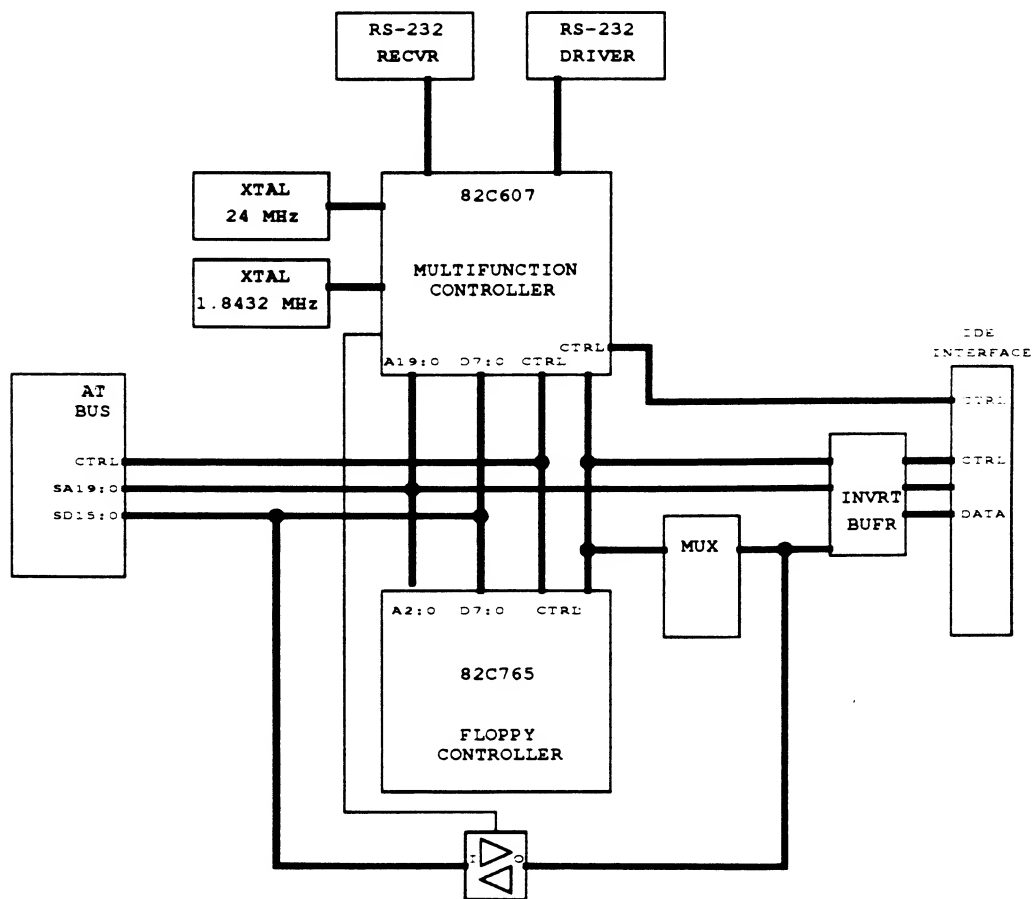
Contains self-calibrated PLL data separator

write-precompensation circuits

logic interface to 765A/765B/8272A FDC

Supports multiple data rates (250K, 300K, & 500Kbps)

---



82C607 Multitfunction Controller

**Manufacturer:** Chips & Technologies

**Processor Supported:** ?

**System Bus:** Micro Channel

**Part:** 82C614, Bus Master Micro Channel Interface Part (MicroCHIP)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

Supports transfer rates up to 20 MB per second

Contains 4 DMA channels with integral FIFO buffer

Supports 32 bit addressing & 16-bit data

Supports data parity checking/generation (MCA)

Supports synchronous CHCK

(4) programmable decode outputs

**Cache:** No

**Clock Speed:** ?

**Main Memory:** No

High speed alternative to DMA slaves

Provides interface to AT bus

Supports streaming data transfers (MCA)

Supports extended POS

Compatible with subsystem control block architecture

Schematic Not Available At Press Time

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286

**System Bus:** AT

**Part:** 82C636, Power Control Unit (part of CS8283 LEAPset CHIPSet)

**Availability:** Q1 1990

**Second Source:** none

**Functions Contained:**

Provides control for CPU, memory, serial ports, modem, display panel backlight, keyboard, & disk drive powers

Stand-by mode support

Manual power on capability

Programmable auto power on by modem rings

Programmable scheduled power on

Slow and normal refresh DRAMs support]

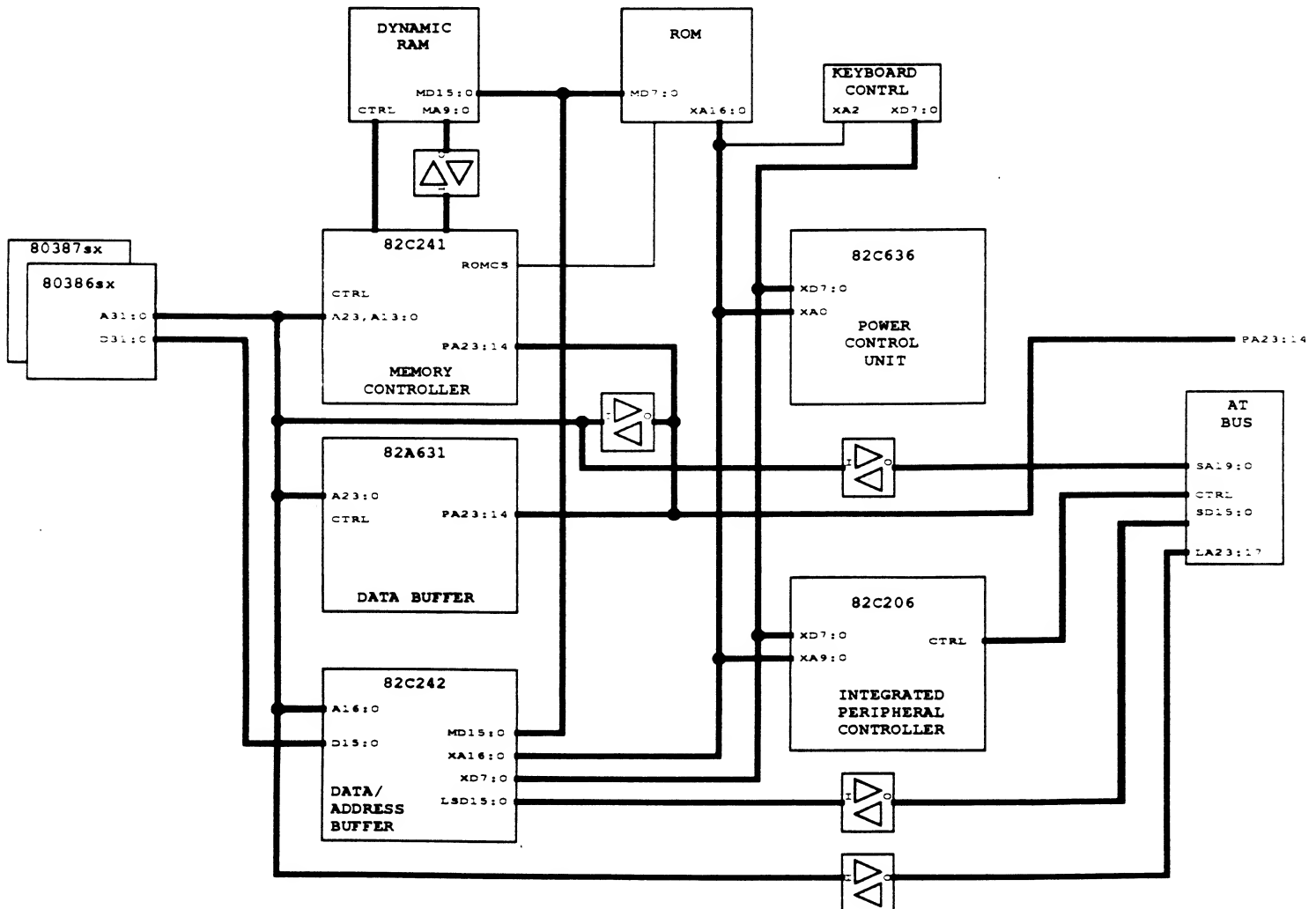
Auto power saving capability with built in programmable timeout counters

(2) multi-purpose programmable parallel I/O ports

**Cache:** No

**Clock Speed:** 12, 16 & 20 MHz

**Main Memory:** No





**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT  
**Part:** 82C641 CHIPS lite, Notebook System Controller  
**Availability:** not yet available  
**Second Source:** none  
**Functions Contained:**  
(2) 8237 compatible DMA Controllers  
(2) 8259 compatible Interrupt Controllers  
(10) 146818 compatible Real Time Clock  
Supports up to 16 MB on-board memory (paged memory support)  
Supports 256 Kb and 1 Mb DRAMs  
Programmable wait states and refresh rates  
Supports 8-bit & 16-bit ROMs  
Supports Shadow RAM  
Supports LIM EMS 4.0 (32 4.0 registers + 4 3.2 registers)  
Supports fast reset and fast GATEA20  
Provides power management features (sleep, stand-by, idle modes)  
Provides graphics interface to CHIPS flat panel controller

---

Schematic Not Available At Press Time

**Manufacturer:** Chips & Technologies

**Processor Supported:** 8088, 80286, 80386

**System Bus:** XT, AT

**Part:** 82C710, Floppy Disk Controller

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Fully mPD72065B and IBM compatible register set

Supports programmable precompensation modes

16 mA PC-XT/AT host interface drive capability

Bi-directional parallel port

Provides PS/2-type mouse port logic & driver support

Contains an analog PLL capable of transfer rates up to 1 Mbps

**Cache:** No

**Clock Speed:** ? MHz

**Main Memory:** No

Provides IDE interface logic

Provides 48 mA floppy driver interface buffers

16450 compatible serial port

Provides general purpose programmable chip select

Provides on-board power management features

Schematic Not Available At Press Time

**Manufacturer:** Chips & Technologies  
**Processor Supported:** 8088, 80286, 80386  
**System Bus:** XT, AT, PS/2 (most)  
**Part:** 82C765, Floppy Disk Controller  
**Availability:** 1989

**Cache:** No  
**Clock Speed:** 24 MHz (XTAL)  
**Main Memory:** No

**Second Source:** none

**Functions Contained:**

Fully mPD765A and IBM-BIOS compatible

On-chip 24 MHz crystal oscillator

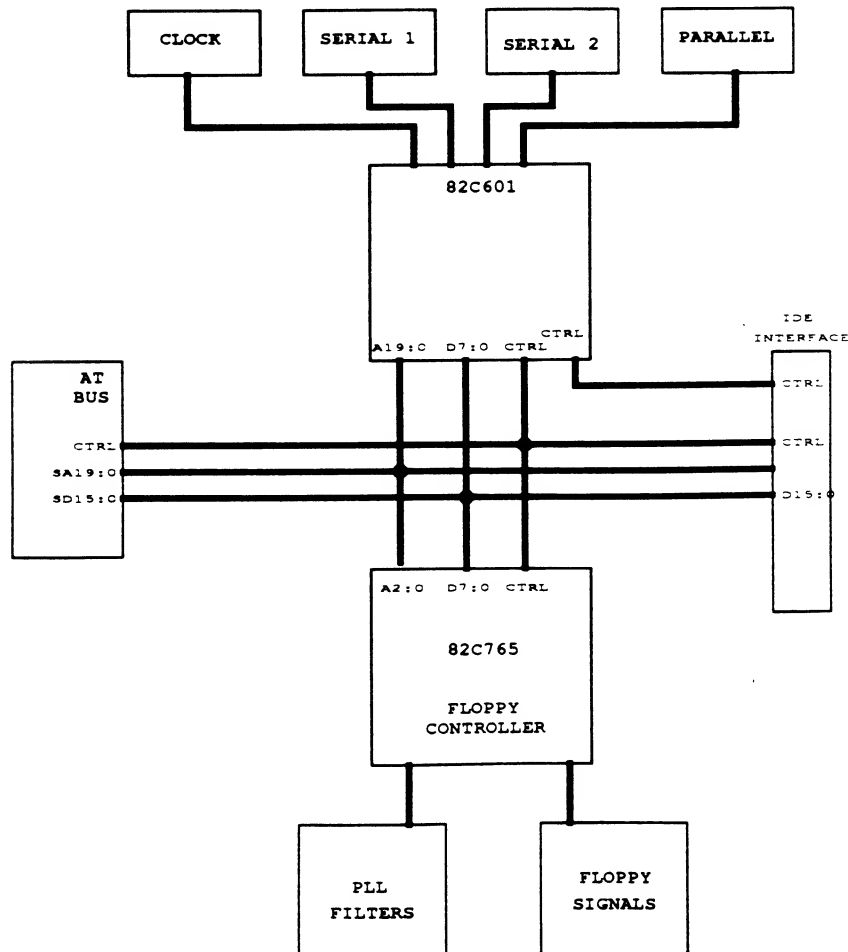
Provides DMA logic, decode of A0-A2, data rate and drive control registers

Data separator with self-calibrating PLL and delay line

Supports write-precompensation

Supports data rates of 1 Mbps and implied seek up to 4000 tracks

Supports IBM and ISO formatting



**Manufacturer:** Chips & Technologies

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82C811, Bus Controller (part of CS8281 NEATsx Data Book)

**Availability:** Q3 1989

**Second Source:** none

**Functions Contained:**

Clock generation with software speed selection

Optional independent AT bus clock

CPU interface and bus control

Programmable command delays and wait state generation

Provides port B registers

---

**Cache:** No

**Clock Speed:** 12 - 16 MHz

**Main Memory:** No

Schematic Not Available At Press Time

**Manufacturer:** Chips & Technologies

**Cache:** No

**Processor Supported:** 80386

**Clock Speed:** 12 - 16 MHz

**System Bus:** AT

**Main Memory:** Yes

**Part:** 82C812, Page/Interleave and EMS Controller (part of CS8281 NEATsx Data Book)

**Availability:** Q3 1989

**Second Source:** none

**Functions Contained:**

Supports page mode access with interleaved memory banks

Supports 100ns DRAMs at 16 MHz page interleaved operation

Supports up to 8 MB on-board memory

Supports 64Kb, 256 Kb, & 1 Mb DRAMs

Provides auto remapping of 640KB - 1 MB RAM to top of 1 MB space

Supports LIM EMS 4.0 address translation logic

Supports shadow RAM of BIOS

Provides staggered refresh (reduces power supply noise)

---

Schematic Not Available At Press Time

**Manufacturer:** Chips & Technologies  
**Processor Supported:** 80386SX  
**System Bus:** AT  
**Part:** 82C836, Single Chip 386sx AT (SCATsx)

**Availability:** Q1 1990

**Second Source:** none

**Functions Contained:**

- (1) 146818 compatible Real Time Clock (RTC)
- (2) 8259 compatible interrupt controllers
- (1) 8255 compatible programmable peripheral interface
- (1) 82288 compatible bus controller decoder)

Supports shadow RAM (8-bit & 16-bit)

Supports LIM EMS 3.2 (4 EMS page registers)

Provides fast gate A20 and fast CPU reset logic

**Cache:** No

**Clock Speed:** up to 20 MHz

**Main Memory:** Yes

- (2) 8237 compatible DMA controllers

- (1) 8254 compatible programmable interval timer

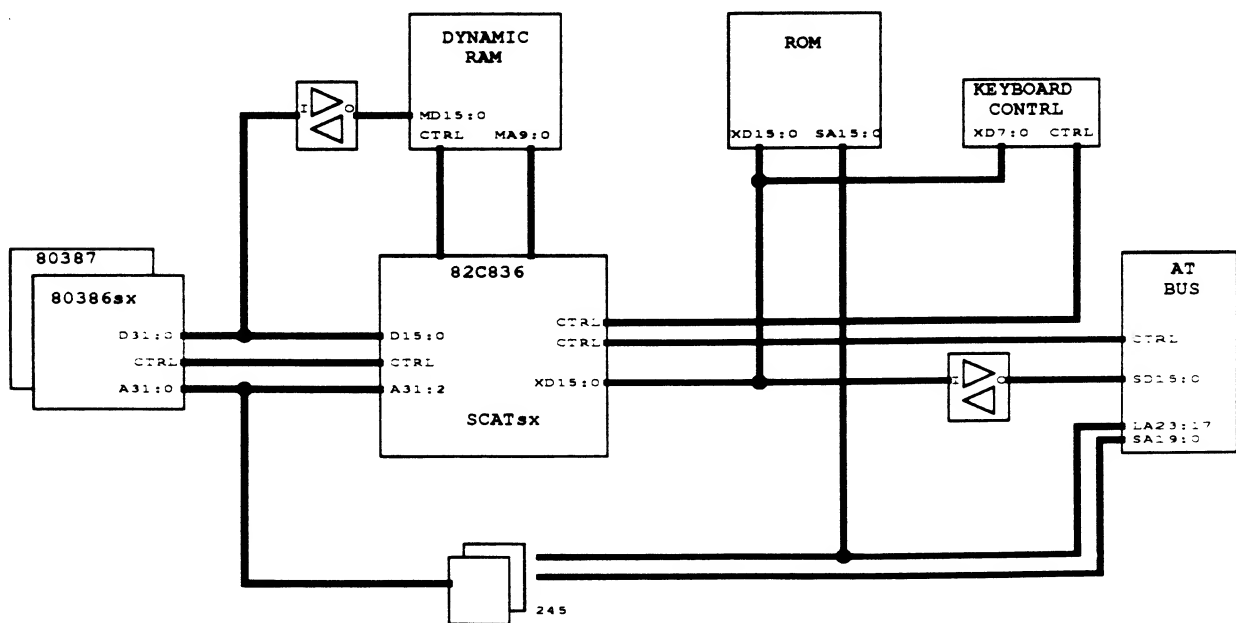
- (1) 82284 compatible clock generation

Supports up to 8 MB of DRAM (16 MB with 74F538

Supports DRAM refresh

Provides 80387sx and 8042 interface logic

Provides power management features



Single Chip 386sx AT (SCATsx) 82C836

**Manufacturer:** Chips & Technologies

**Processor Supported:** 80286,80386

**System Bus:** AT

**Part:** 82C3785, Single Chip PC-AT Hard Disk Controller

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

100% IBM PC/AT Task File Support

Auto-generated wait states for fast hosts

Supports disk data rates up to 24 Mbps

Supports 16-bit CRC & 32/56-bit ECC

Supports daisy chaining two embedded drives

Supports 10 MB per second buffer throughput

Auto-command mode (improves disk command response)

Optional auto-increment of address pointer for local CPU to buffer access

---

**Cache:** No

**Clock Speed:** ? MHz

**Main Memory:** No

24mA drivers for direct AT interface

PIO and DMA modes for data transfers up to 8 MB per second

Optional dual brand registers

Provides on-board power management features

Provides control for 64KB dual port SRAM buffer

Provides programmable disk sequencer RAM (30 x 4 bytes)

Schematic Not Available At Press Time





**Manufacturer:** Cyrix Corp.

**Cache:** No

**Processor Supported:** 80386SX

**Clock Speed:** 16, 20 & 25 MHz

**System Bus:** AT

**Main Memory Support:** No

**Part:** CX-83S87 FastMath Coprocessor, High Performance CMOS Math Processor

**Availability:** 1990

**Second Source:** pin/software compatible with Intel 80387SX NCP

**Functions Contained:**

Zero wait state read operations

Low power dissipation

Single input clock for all designs

Implements extended double precision IEEE-754

---

Schematic Not Available At Press Time

**Manufacturer:** Cyrix Corp.

**Processor Supported:** 80386SX/DX

**System Bus:** AT

**Part:** FastMath CX-83D87 Coprocessor

**Availability:** 1990

**Second Source:** socket/software compatible with Intel 80387

**Functions Contained:**

Optional memory-mapped interface

Requires 4 to 10 times fewer clock FastMath than 80387

ESD protection & latch up prevention logic

Implements extended double precision IEEE-754-1990

Faster transcendental function evaluation

---

**Cache:** No

**Clock Speed:** 16, 20, 25, 33 & 40MHz

**Main Memory Support:** No

**Schematic Not Available At Press Time**

**Manufacturer:** Cyrix Corp.

**Processor Supported:** 80386SX/DX

**System Bus:** AT

**Part:** EMC87, Ultra High Performance Coprocessor

**Availability:** 1990

**Second Source:** software compatible with Intel 80387

**Functions Contained:**

Interfaces with the 80386 via 121 pin EMC socket

Optional memory-mapped interface

Requires 4 to 10 times fewer clock FastMath than 80387

ESD protection & latch up prevention logic

Implements extended double precision IEEE-754-1990

Faster transcendental function evaluation

---

**Cache:** No

**Clock Speed:** 20, 25 & 33 MHz

**Main Memory Support:** No

Schematic Not Available At Press Time



**Manufacturer:** Edsun Laboratories Inc.

**Processor Supported:** 8088, 80286

**System Bus:** XT/AT

**Part:** EL286-88, 80286 to 8088 Processor Signal Converter

**Availability:** 1985

**Second Source:**

**Functions Contained:**

Translates control signal and 16-bit transfer sequences from 80286 to multiple 8-bit 8088 sequence

Hardware selectable memory ranges

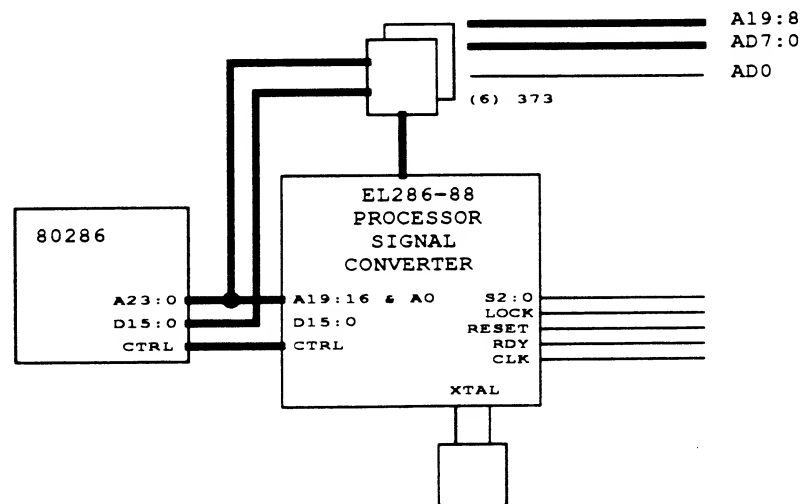
Separate 8088 clock for asynchronous operations

DMA support for IBM-PC retro fit 80286

**Cache:** No

**Clock Speed:** 8 MHz

**Main Memory Support:** No



Edsun 80286 to 8088 Processor Signal Converter

**Manufacturer:** Elite Microelectronics Inc.

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** e88C311CPU/Cache/DRAM Controller (part of Eagle chipset)

**Availability:** 1991

**Second Source:**

**Functions Contained:**

Supports direct mapped or 2-way set associative

Supports pipelined & non-piplined operation

Supports from 1MB to 64MB on board memory

Provides page and 2-way/4-way page interleaving

Permits ZERO wait states during cache miss/page

Supports hidden, burst & PC-AT style refresh

**Cache:** Yes

**Clock Speed:** 25 & 33 MHz

**Main Memory Support:** Yes

0 wait state, buffered write through DRAM update

Supports 256K-, 1M-, & 4M-bit DRAMS

Supports 256KB shadow RAM with 16KB granularity

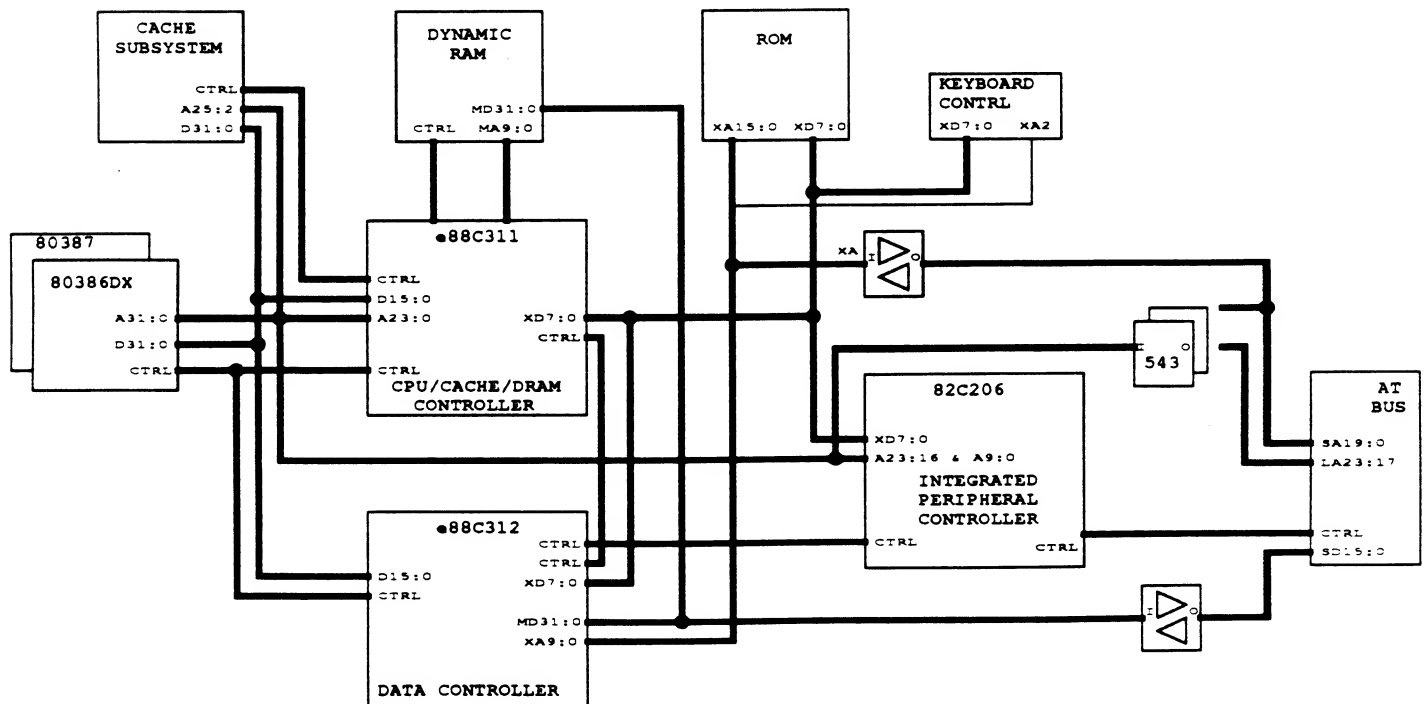
Supports 32KB, 64KB and 128KB cache memory

Allows remapping of memory (4 blocks from 4KB to 4MB)

**Schematic Not Available At Press Time**

**Manufacturer:** Elite Microelectronics Inc.  
**Processor Supported:** 80386DX  
**System Bus:** AT  
**Part:** e88C312 Data Controller (part of Eagle chipset)  
**Availability:** 1991  
**Second Source:**  
**Functions Contained:**  
 Supports 80387 and Weitek WTL3167  
 Fast GATEA20 & Fast Reset for OS/2  
 On-board chip selection logic for (2) serial & (1) parallel port  
 On-board chip selection logic for (2) programmable I/O ports

**Cache:** Yes  
**Clock Speed:** 25 & 33 MHz  
**Main Memory Support:** Yes



Elite Eagle Chipset

\* CACHE SUBSYSTEM CONTAINS  
 SRAM AND BUFFERS

**Manufacturer:** Electronics Research & Development Co.

**Processor Supported:** 8088, 8026, 80386SX

**System Bus:** XT

**Part:** Arjun, Peripheral Controller

**Availability:** ?

**Second Source:** ?

**Functions Contained:**

6845 compatible CGA (ASCII & Russian ROM)

(1) printer port with readback facility

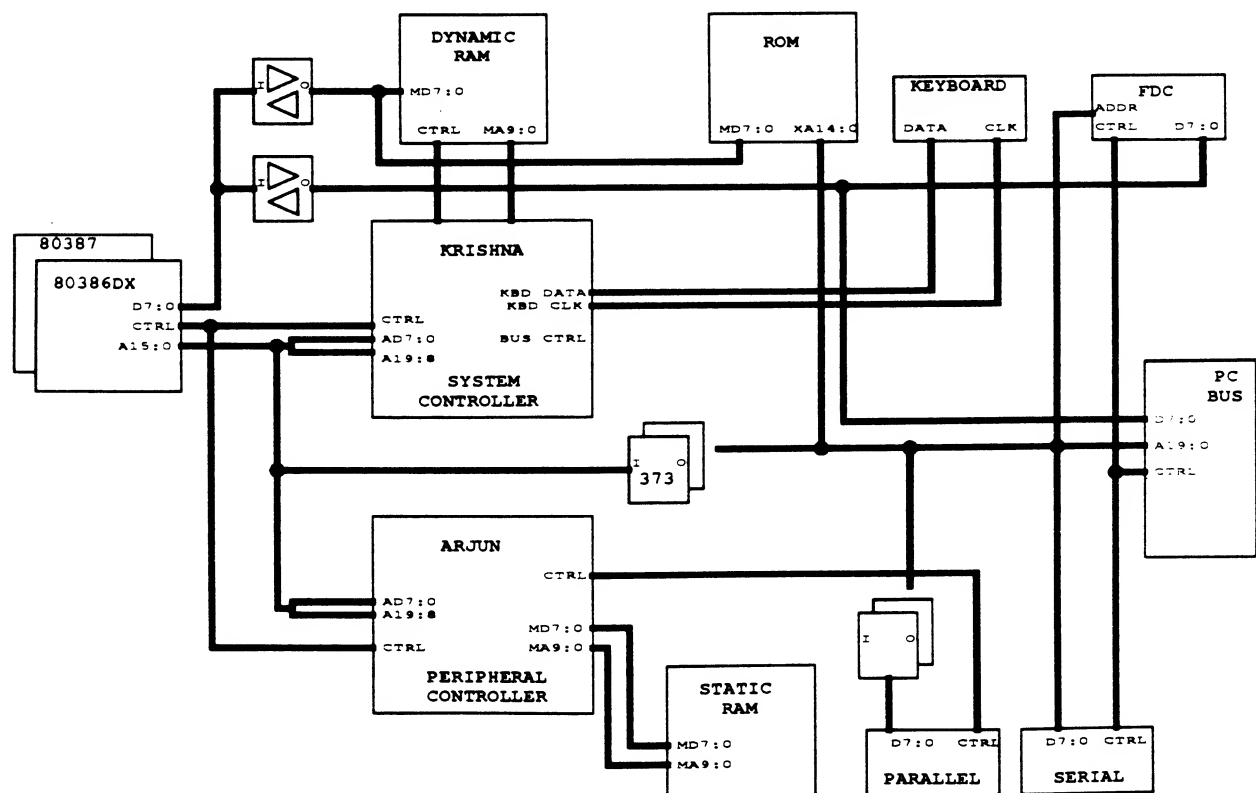
50 bytes of battery backed static RAM

**Cache:** No

**Clock Speed:** up to 20 MHz

**Main Memory Support:** No

(1) 8250 compatible serial port  
Battery-backed Real Time Clock  
light pen interface



ERDC Krishna & Arjun XT Chipset



**Manufacturer:** Electronics Research & Development Co.

**Processor Supported:** 8088

**System Bus:** XT

**Part:** Krishna, Multifunction System Controller

**Availability:** ?

**Second Source:** ?

**Functions Contained:**

Generates all bus control signals

(1) 8237 compatible DMA controller

(1) 8259 compatible Programmable Interrupt Controller

Parity generation/checking circuitry

Supports shadow RAM

Supports 256K, 512K and 640K on-board memory

**Cache:** No

**Clock Speed:** 4.77, 7.15 & 9.54 MHz

**Main Memory Support:** Yes

Generates all transceiver control signals

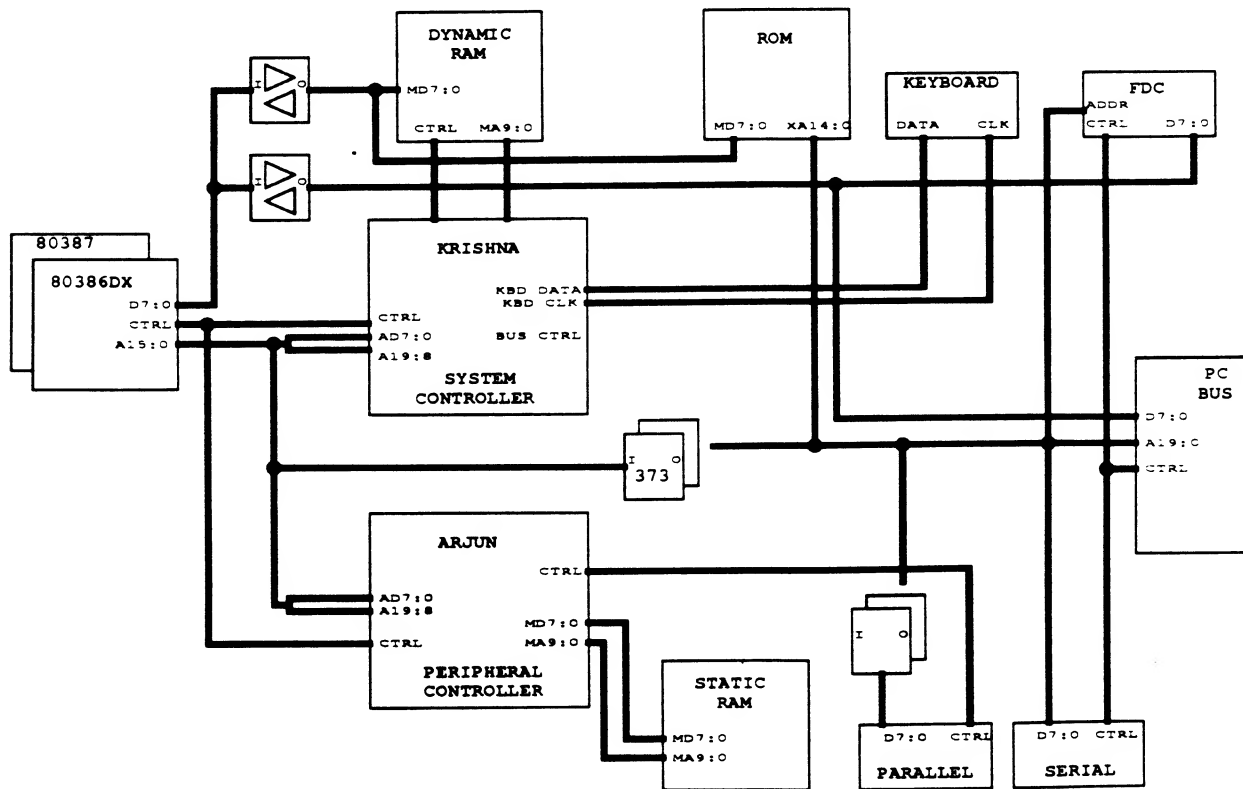
(1) 8254 compatible Programmable Timer

Direct keyboard interface circuitry

NMI control logic

Supports 1M bit x1 DRAM

Supports 64KB ROM



ERDC Krishna & Arjun XT Chipset

**Cache: No**

**Clock Speed:** ? MHz

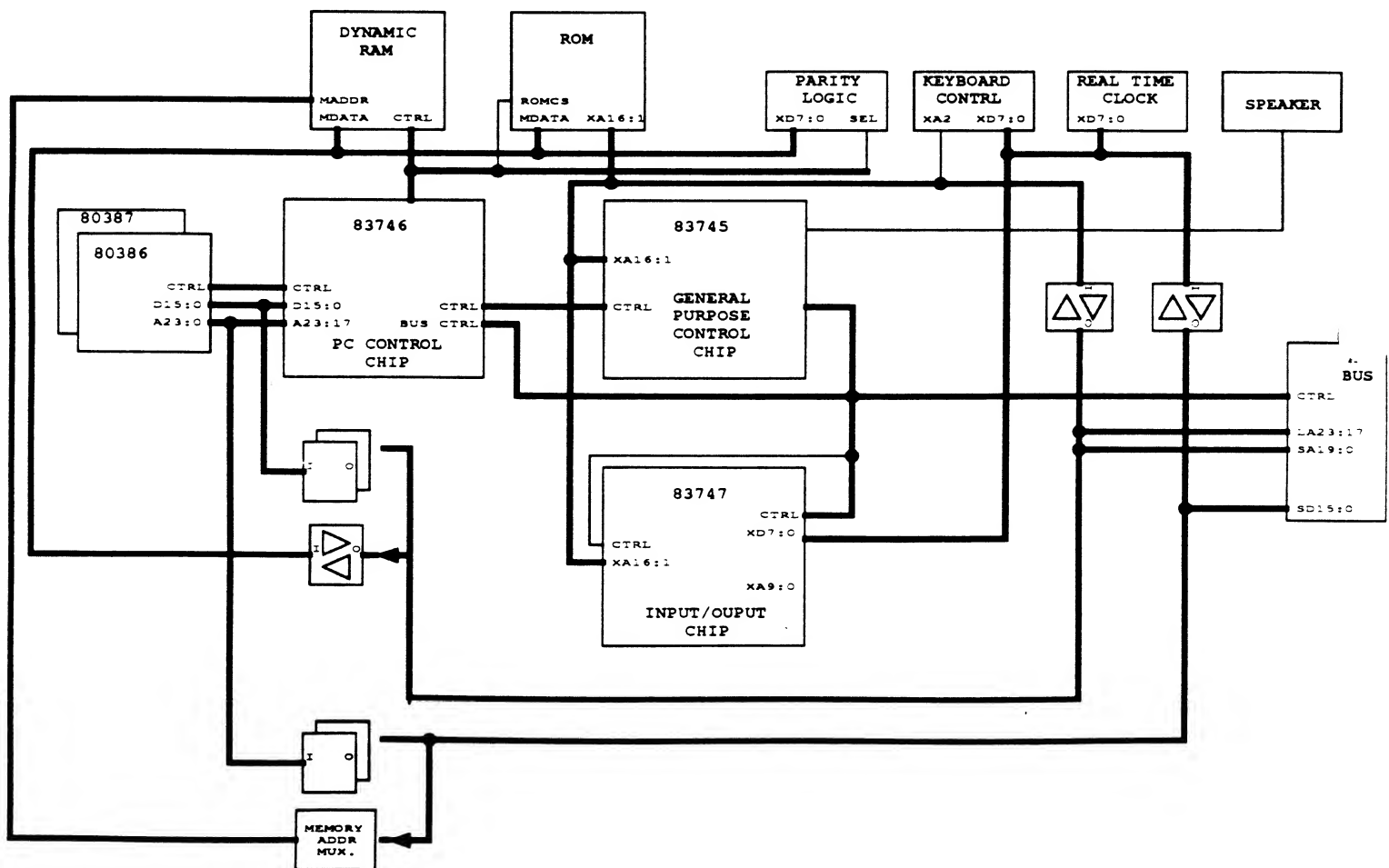
**Main Memory Support:** No

**(2) 8259 compatible Interrupt Controller**

(1) 8284 compatible

Provides NMI generation logic

### Wait state generation



ERSO PC/AT Chipset

**Manufacturer:** Electronics Research & Service Organization

**Processor Supported:** 80286

**System Bus:** AT

**Part:** CIC 83746, Personal Computer Control Chip

**Availability:** ?

**Second Source:**

**Functions Contained:**

Replaces 82288 bus controller

Generates system clock

Provides data conversion logic

System board memory address decode

8 MHz system clock zero wait state, 120ns DRAM

Provides commands & control signal for local & system bus

**Cache:** No

**Clock Speed:** ? MHz

**Main Memory Support:** No

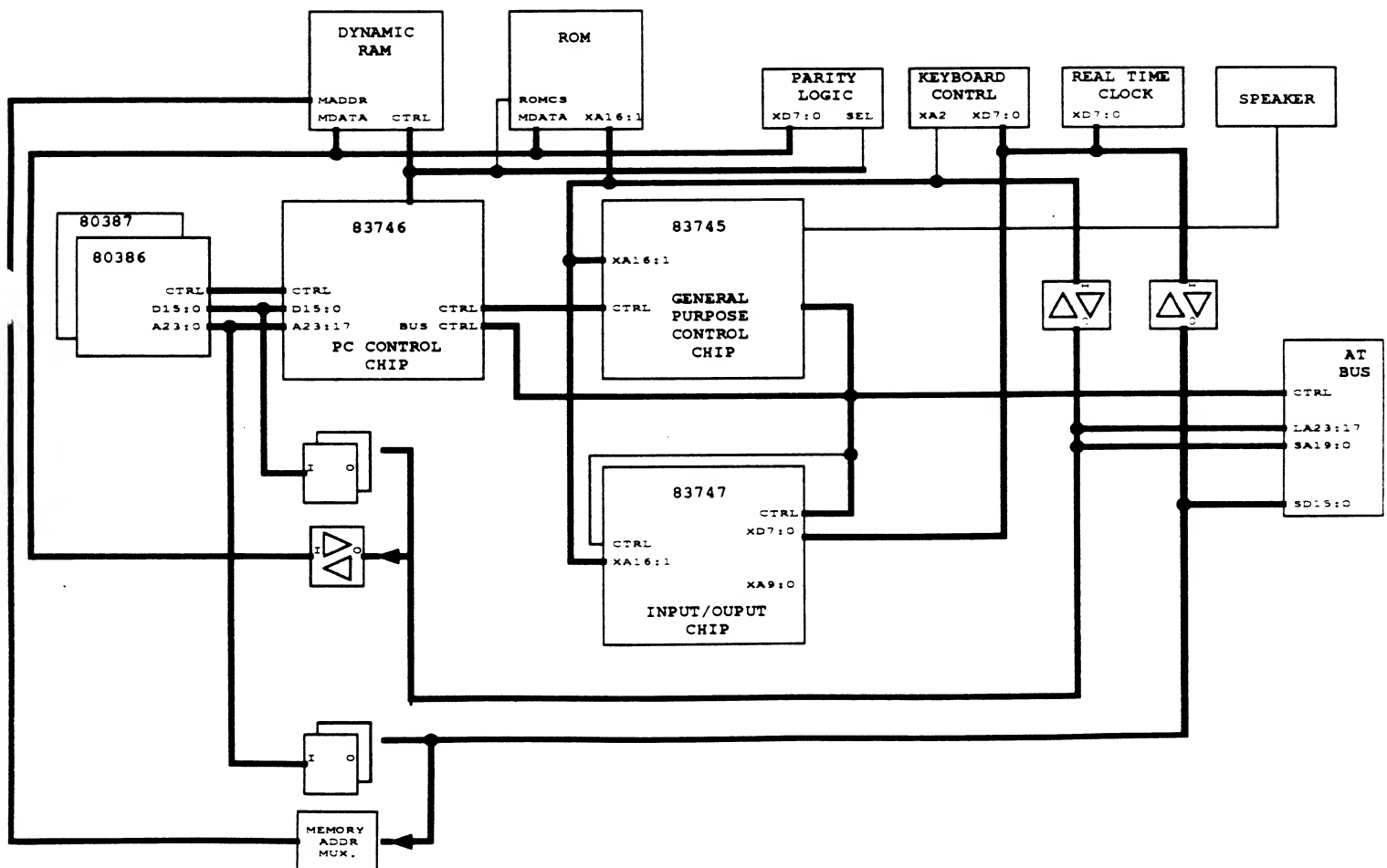
Replaces 82284

Generates system, CPU and NCP reset signals

Provides variable wait stat selection

Numeric Processor interface signals

10 MHz system clock one wait state, 120ns DRAM



ERSO PC/AT Chipset

## Personal Computer Design

**Manufacturer:** Electronics Research & Service Organization

**Processor Supported:** 80286

**System Bus:** AT

**Part:** CIC 83747, Input/Output Chip

**Availability:** ?

**Second Source:**

**Functions Contained:**

(2) 16450 compatible Serial UARTs

Provides full double buffering

Fully prioritized interrupt system controls

**Cache:** No

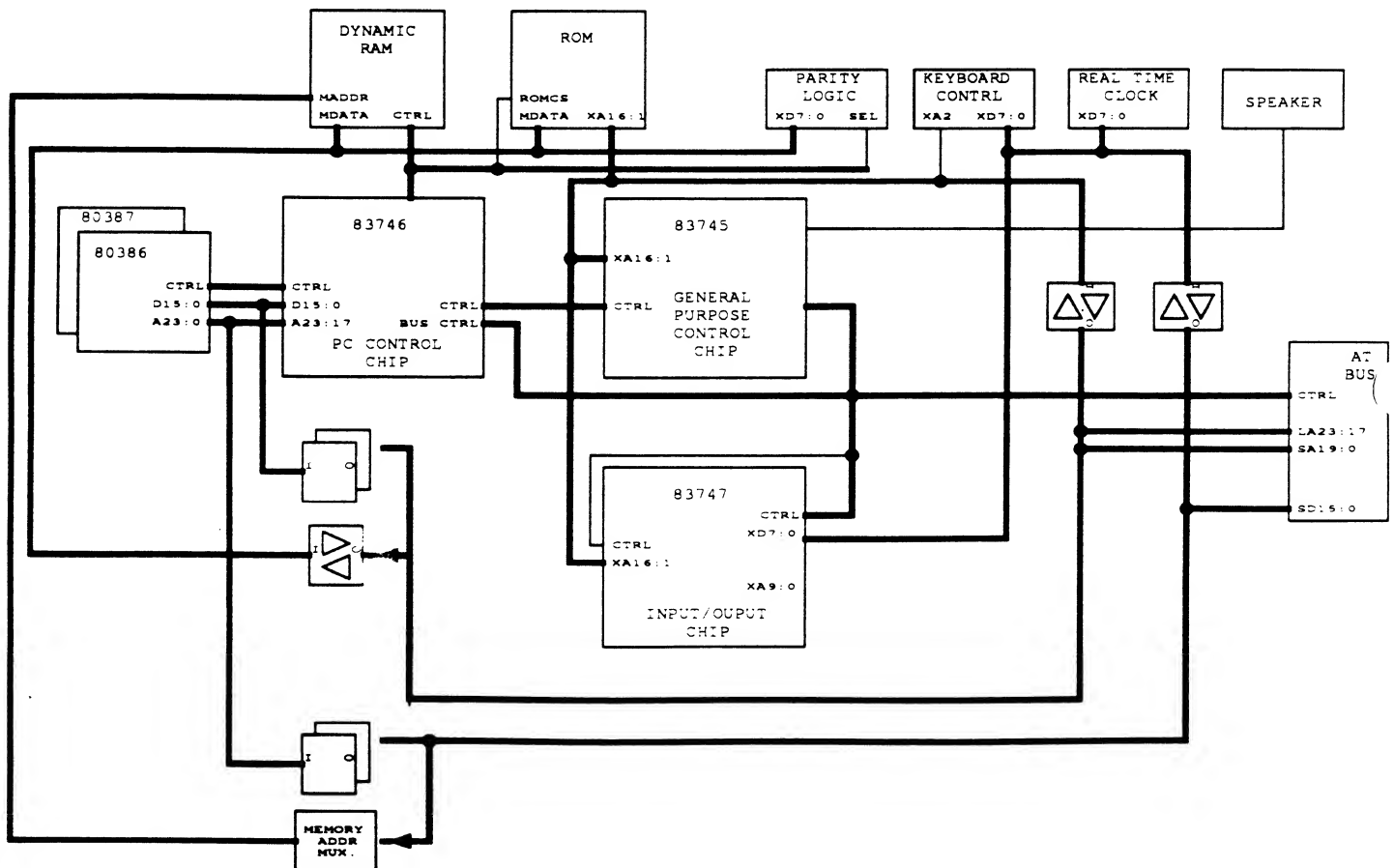
**Clock Speed:** ? MHz

**Main Memory Support:** No

Supports modem control functions

Provides programmable baud-rate generator

(2) Parallel ports



ERSO PC/AT Chipset

**Manufacturer:** G-2 Incorporated

**Processor Supported:** 80286

**System Bus:** AT

**Part:** HTGC101, Peripheral Controller (part of 12/16 MHz PC/AT Compatible Chipset)

**Availability:** 1987

**Second Source:** none

**Functions Contained:**

Supports 256K and 1M bit DRAMs

(1) MF82284 compatible clock generator

(1) MF82288 compatible I/O command generator

(2) MF8237 compatible DMA Controllers

MF = megafunction

**Cache:** No

**Clock Speed:** up to 16 MHz

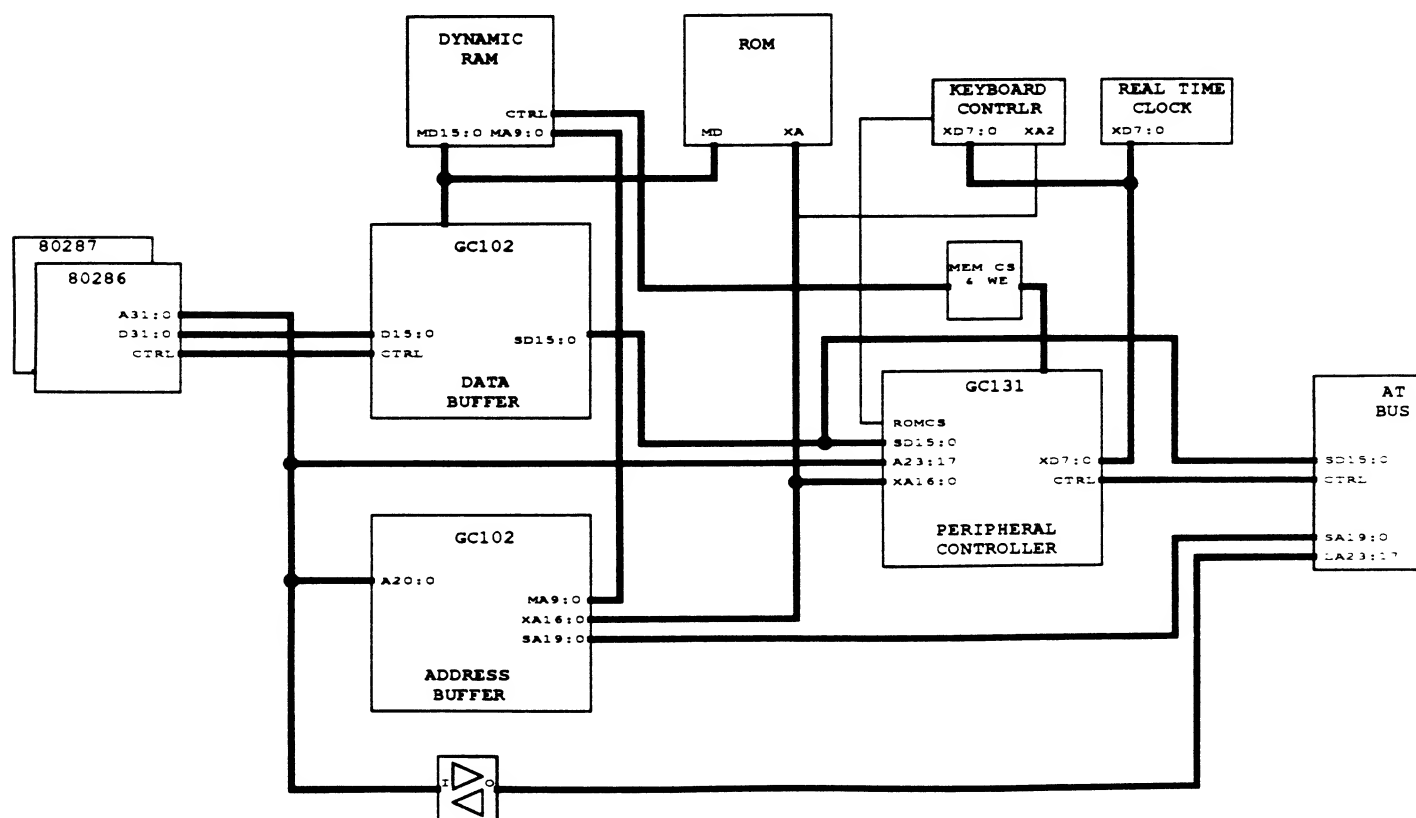
**Main Memory Support:** Yes

Supports up to 4MB on-board memory

(1) MF74612 compatible Memory Mapper

(1) MF8254 compatible Programmable Timer

(2) MF8259 compatible Interrupt Controllers



G2 AT Compatible 80386 3 Chipset

## Personal Computer Design

**Manufacturer:** G-2 Incorporated

**Processor Supported:** 80286

**System Bus:** AT

**Part:** HTGC102, Address/Data Buffer (part of 12/16 MHz PC/AT Compatible Chipset)

**Availability:** 1987

**Second Source:** none

**Functions Contained:**

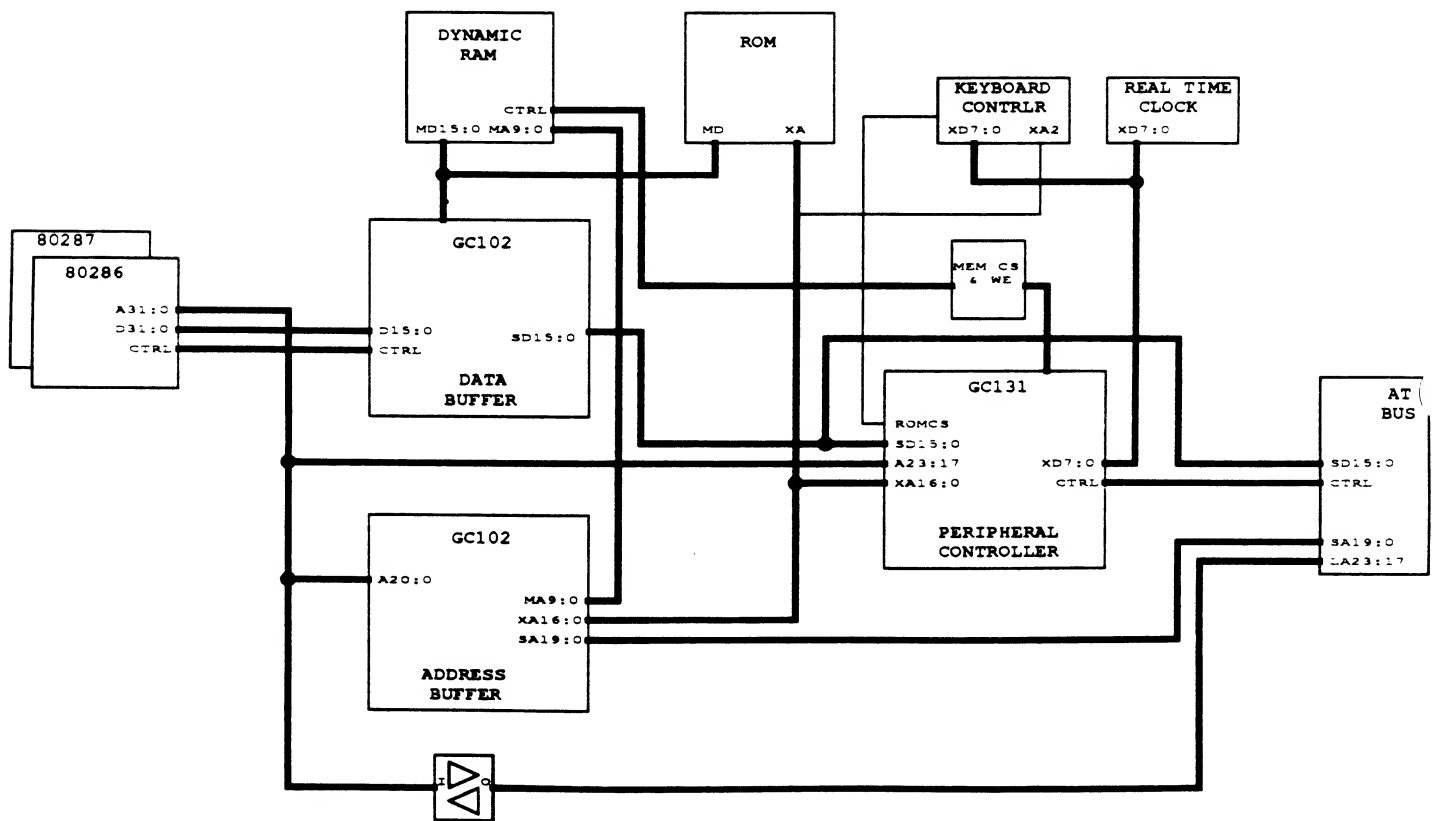
Configured as either address or data buffers

Replaces buffers, data transceivers, memory drivers, parity generators and supporting circuitry

**Cache:** No

**Clock Speed:** up to 16 MHz

**Main Memory Support:** Yes



G2 AT Compatible 80386 3 Chipset

**Manufacturer:** G2 Inc..

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** GC131, Peripheral Controller (part of AT compatible 386 Chip Set)

**Availability:** 1988

**Second Source:** none

**Functions Contained:**

Provides AT compatible parity and NMI control

Supports direct connection of 8042 (kbd ctrlr)

Supports external EEPROM

(1) 82284 compatible clock generator

(1) 8284 compatible OSC Clock generator

(2) 8237 compatible DMA Controllers

**Cache:** No

**Clock Speed:** 20 MHz

**Main Memory Support:** No

Supports shadow RAM

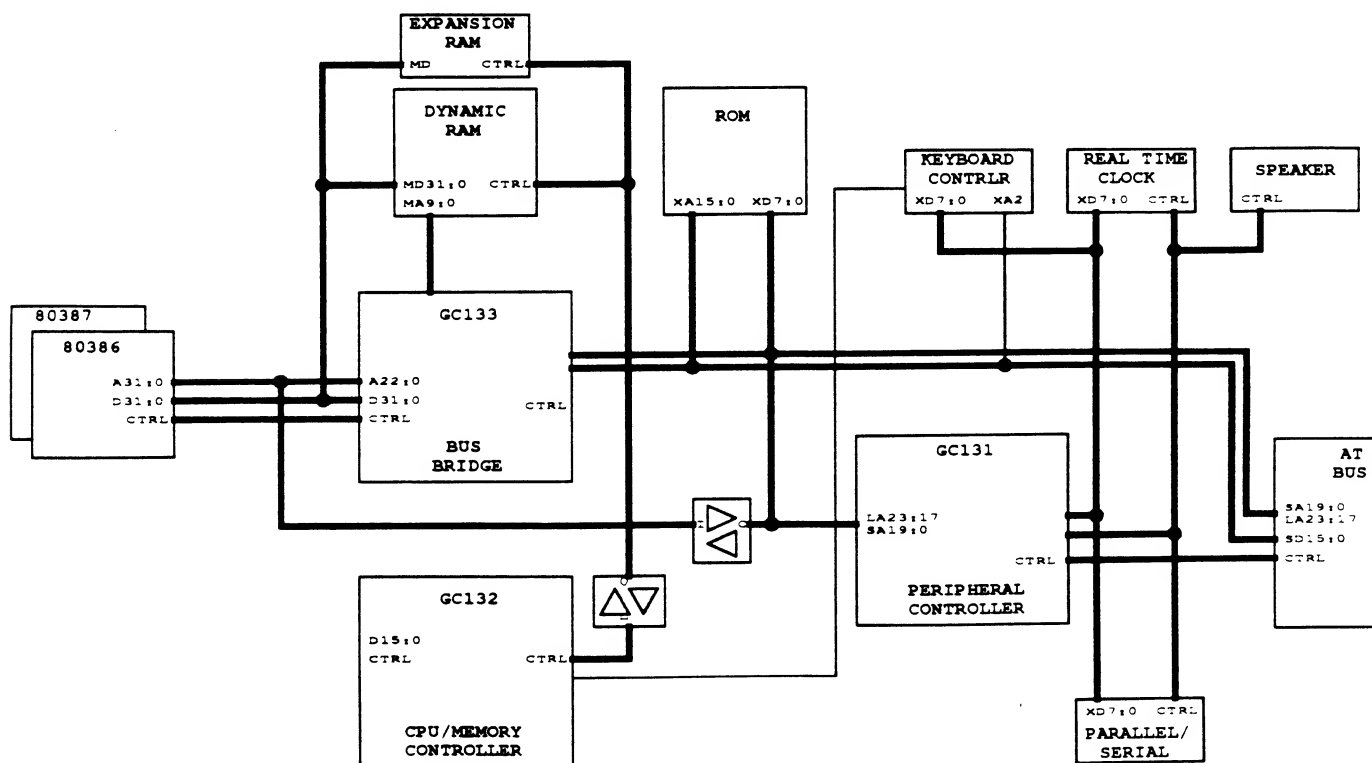
Provided chip selects for 2 serial & 1 parallel ports

Contains software accessible registers

(1) 74612 compatible Memory Mapper

(1) 8254 compatible Programmable Timer

(2) 8259 compatible Interrupt Controllers



G2 AT Compatible 80386 3 Chipset

**Manufacturer:** G2 Inc..

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** GC132, CPU/Memory Controller (part of AT compatible 386 Chip Set)

**Availability:** 1988

**Second Source:** none

**Functions Contained:**

Provides functions of system bus, DRAM, clock and reset control

Provides AT bus control signals from processor requests

Logic for clock generation, speed selection, and reset to synchronize with 80386 and math coprocessor

Shutdown detection and action

Supports variable DRAM timing

Supports up to 24MB DRAM

Supports both 80387 and 80287

Supports parity detection and generation

**Cache:** No

**Clock Speed:** 20 MHz

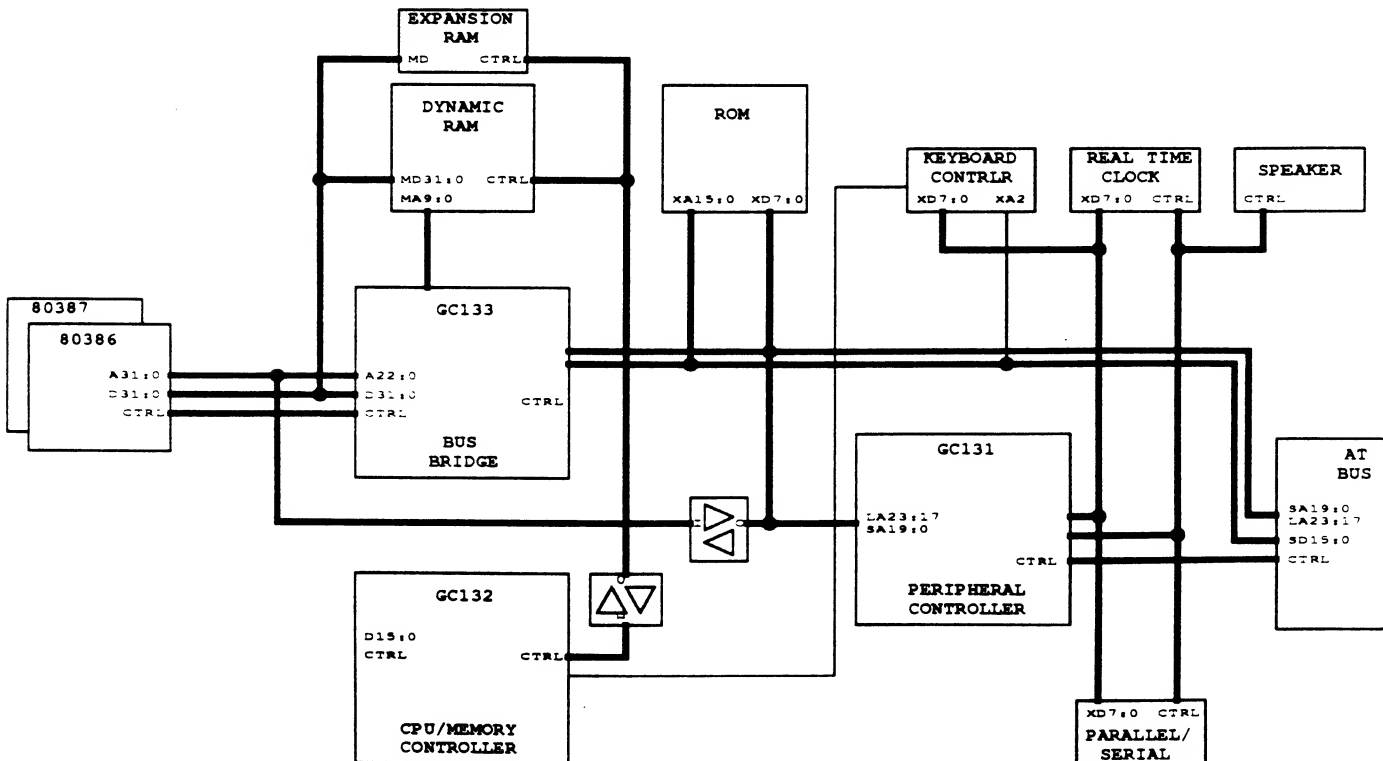
**Main Memory Support:** Yes

Supports six banks of SRAM or DRAM

Supports 256K or 1M bit DRAMs

Converts 16-bit bus to 8-bit AT bus

Supports shadow RAM



G2 AT Compatible 80386 3 Chipset



**Manufacturer:** G2 Inc..

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** GC133, Bus Bridge (part of AT compatible 386 Chip Set)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Provides a bridge between 32-bit CPU data and 16-bit AT-compatible bus

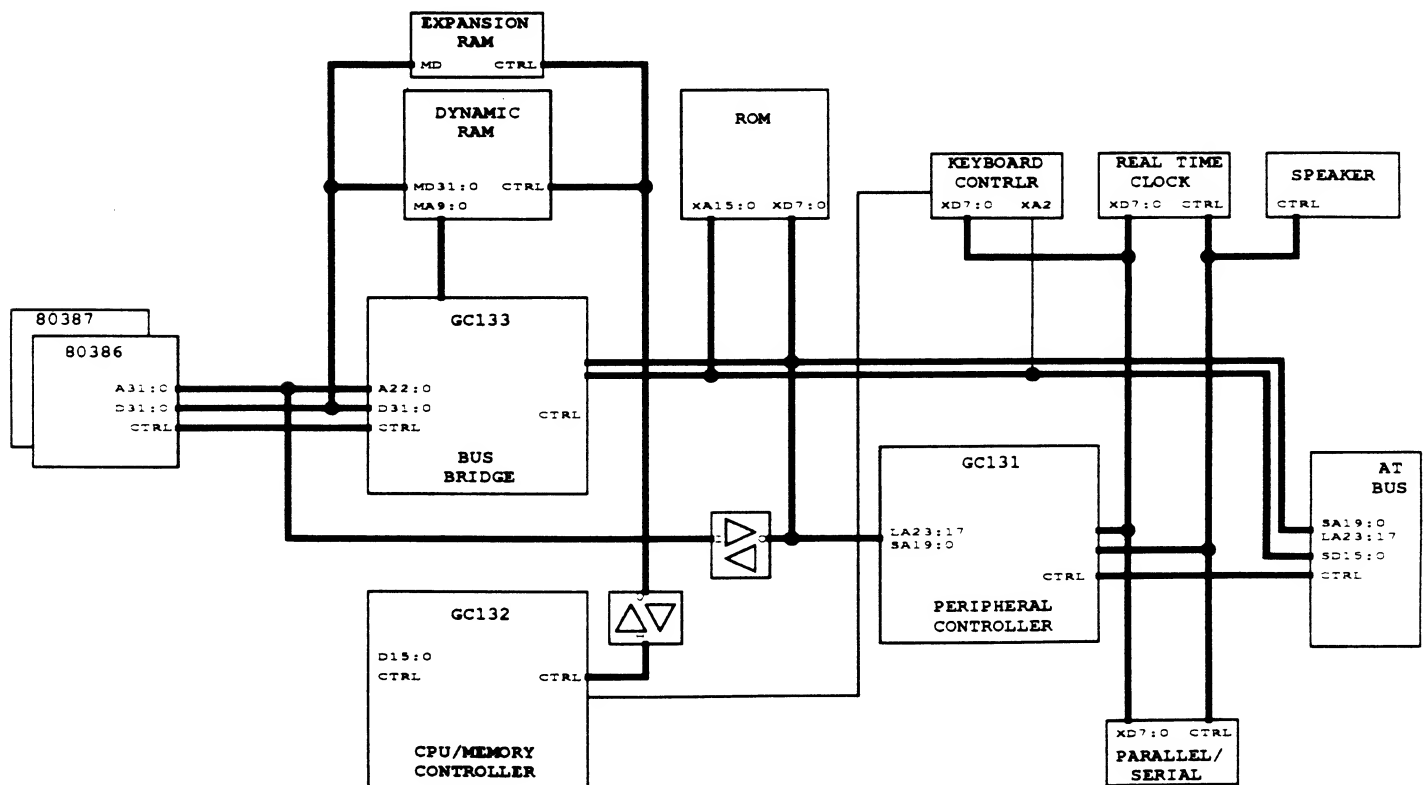
Provides Address latch and Memory address multiplexer

Page mode violation detection

**Cache:** No

**Clock Speed:** 20 MHz

**Main Memory Support:** Yes



G2 AT Compatible 80386 3 Chipset



**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 8088

**System Bus:** XT

**Part:** HT10, Super XT Chip

**Availability:** ?

**Second Source:**

**Functions Contained:**

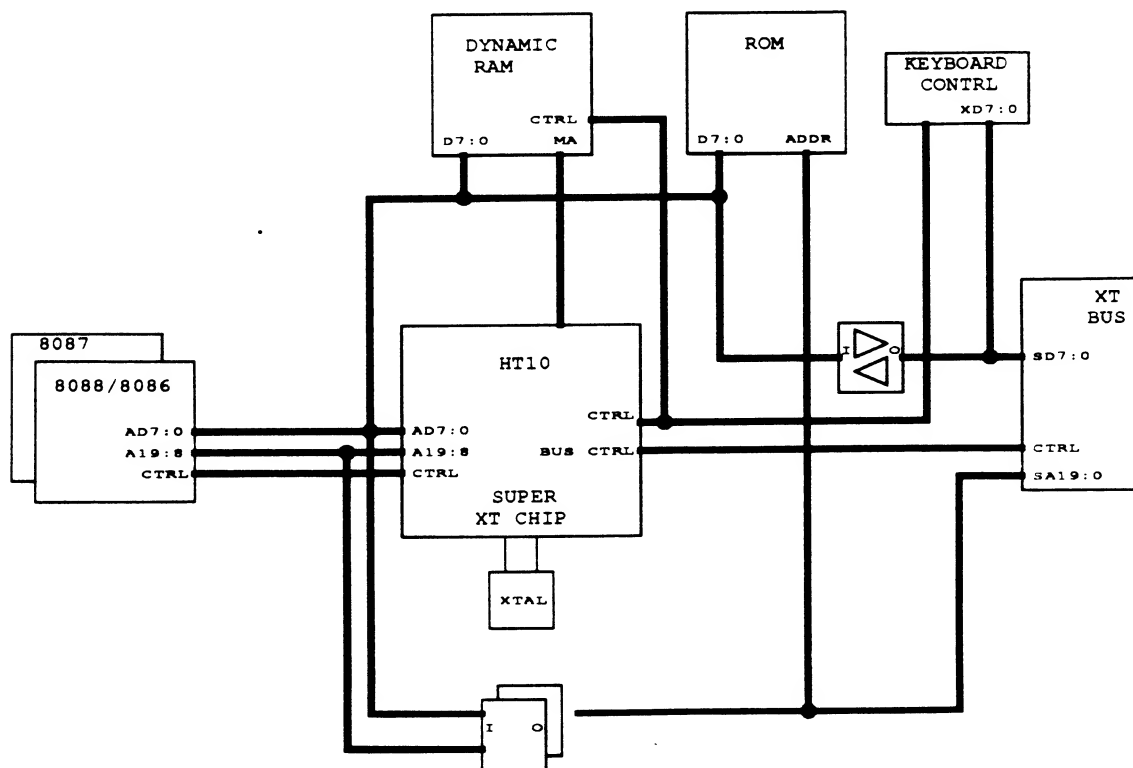
Supports 256K and 1M DRAMs at zero or one wait state Supports 8- and 16-bit data widths

Integrates functions of DMS, timers, peripheral interface, interrupt and bus controllers and support circuitry

**Cache:** No

**Clock Speed:** up to 10 MHz

**Main Memory Support:** No



Headland XT Compatible Single Chip

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80286

**System Bus:** AT

**Part:** HT12, Single 286 AT Chip

**Availability:** 1989

**Second Source:**

**Functions Contained:**

Supports up to 4 MB on-board memory

(1) 82284 compatible clock generator

(1) 8284 compatible OSC Clock generator

(2) 8237 compatible DMA Controllers

Supports shadow RAM (system and video)

Supports 384K remapping

**Cache:** No

**Clock Speed:** up to 16 MHz

**Main Memory Support:** Yes

Supports 64K, 256K, and 1M DRAM in mixed mode

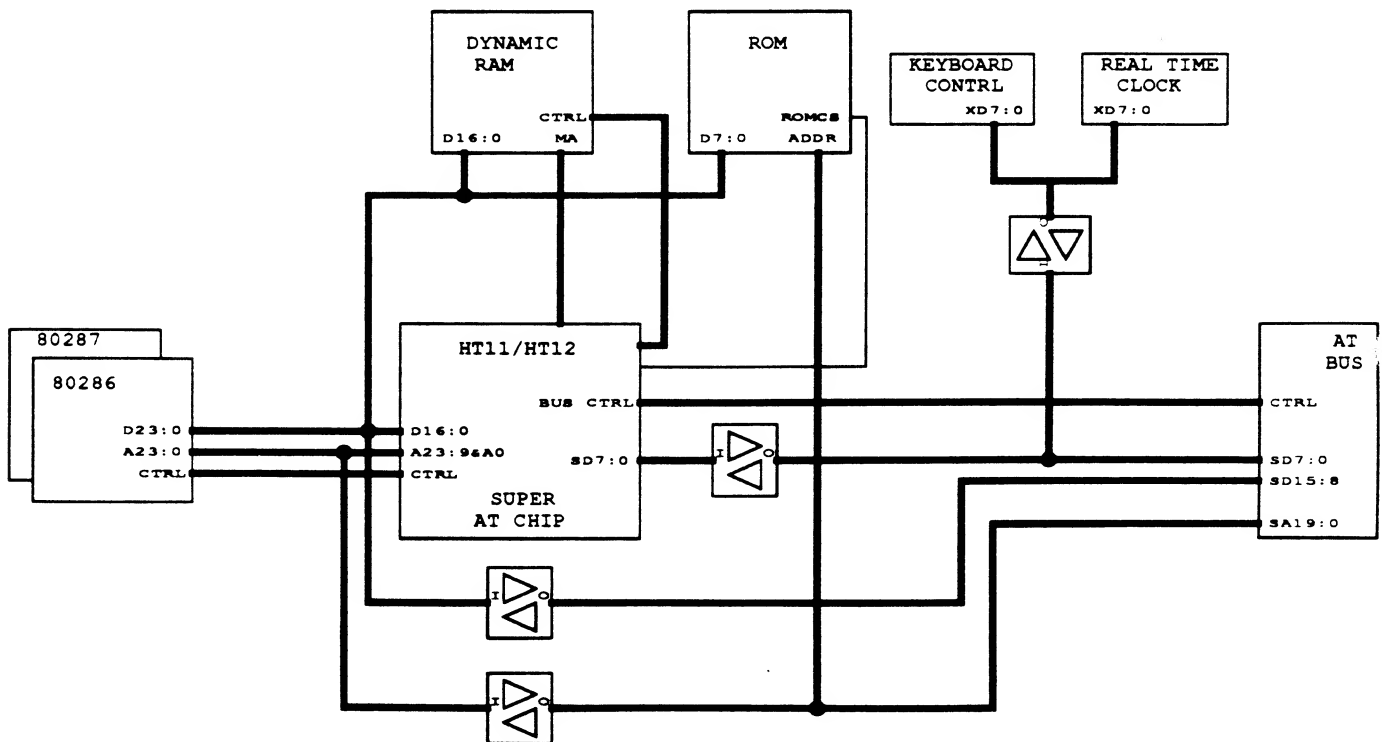
(1) 74612 compatible Memory Mapper

(1) 8254 compatible Programmable Timer

(2) 8259 compatible Interrupt Controllers

Supports LIM EMS 4.0 with 4 registers

Provides Port 92, hot reset and fast A20Gate



Headland AT Compatible Single Chip

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** HT15, ISA/386SX System Chip

**Availability:** 1990

**Second Source:**

**Functions Contained:**

Supports pipelined mode

Supports up to 16 MB in 4 banks on-board memory

Supports combined video and system BIOS

Supports shadow RAM (system and video)

Supports 384K remapping

(1) 82284 compatible clock generator

(1) 8284 compatible OSC Clock generator

(2) 8237 compatible DMA Controllers

**Cache:** No

**Clock Speed:** up to 20 MHz

**Main Memory Support:** Yes

Supports true zero wait state DRAM access

Supports 64K, 256K, and 1M DRAM in mixed mode

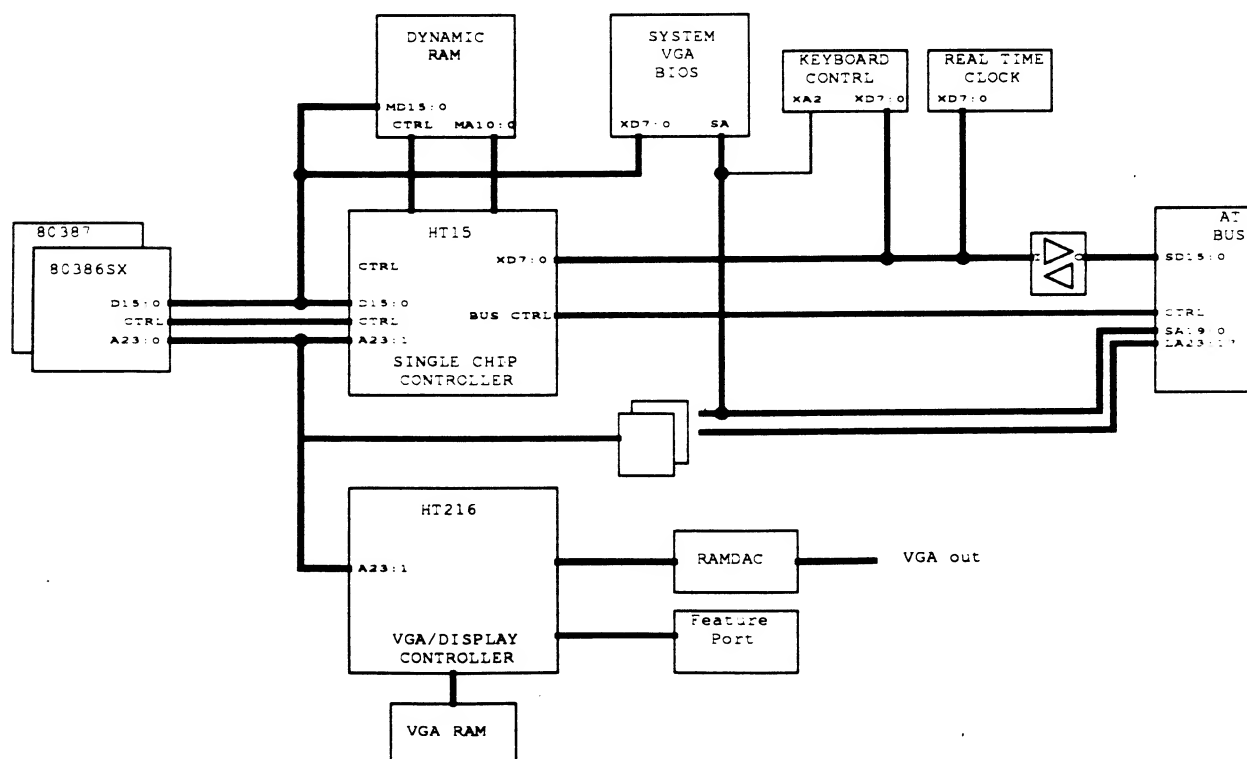
Supports LIM EMS 4.0 with 4 registers

Provides Port 92, hot reset and fast A20Gate

(1) 74612 compatible Memory Mapper

(1) 8254 compatible Programmable Timer

(2) 8259 compatible Interrupt Controllers



Headland HT15 386SX AT Compatible Single Chip

**Manufacturer:** Headland Technology Inc.  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT  
**Part:** HT21, PC/AT Compatible Single Chip  
**Availability:** 1990

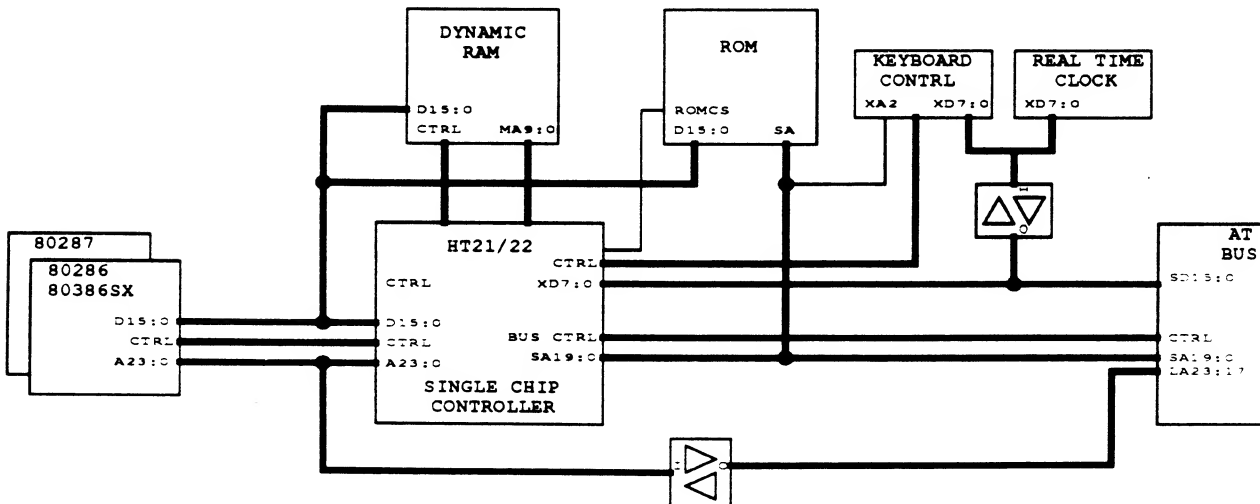
**Second Source:**

**Functions Contained:**

Supports pipeline mode operation  
Supports up to 8 MB on-board memory  
Page mode and 2-way/4-way interleaving  
Supports LIM EMS 4.0 (2 sets of 32 registers)  
(1) 82284 compatible clock generator  
(1) 8284 compatible OSC Clock generator  
(2) 8237 compatible DMA Controllers  
Supports combined video and system BIOS

**Cache:** No  
**Clock Speed:** 16 & 20 MHz  
**Main Memory Support:** Yes

Supports 12 MHz backplane operation  
Supports 256K and 1M DRAMs  
8-bit or 16-bit BIOS support  
Provides hot reset and fast A20Gate  
(1) 74612 compatible Memory Mapper  
(1) 8254 compatible Programmable Timer  
(2) 8259 compatible Interrupt Controllers  
Supports shadow RAM (system and video)



Headland HT21/22 386SX / 286 AT Compatible Single Chip

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** HT101SX, Peripheral Controller (part of HTK113SX Chip Set)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

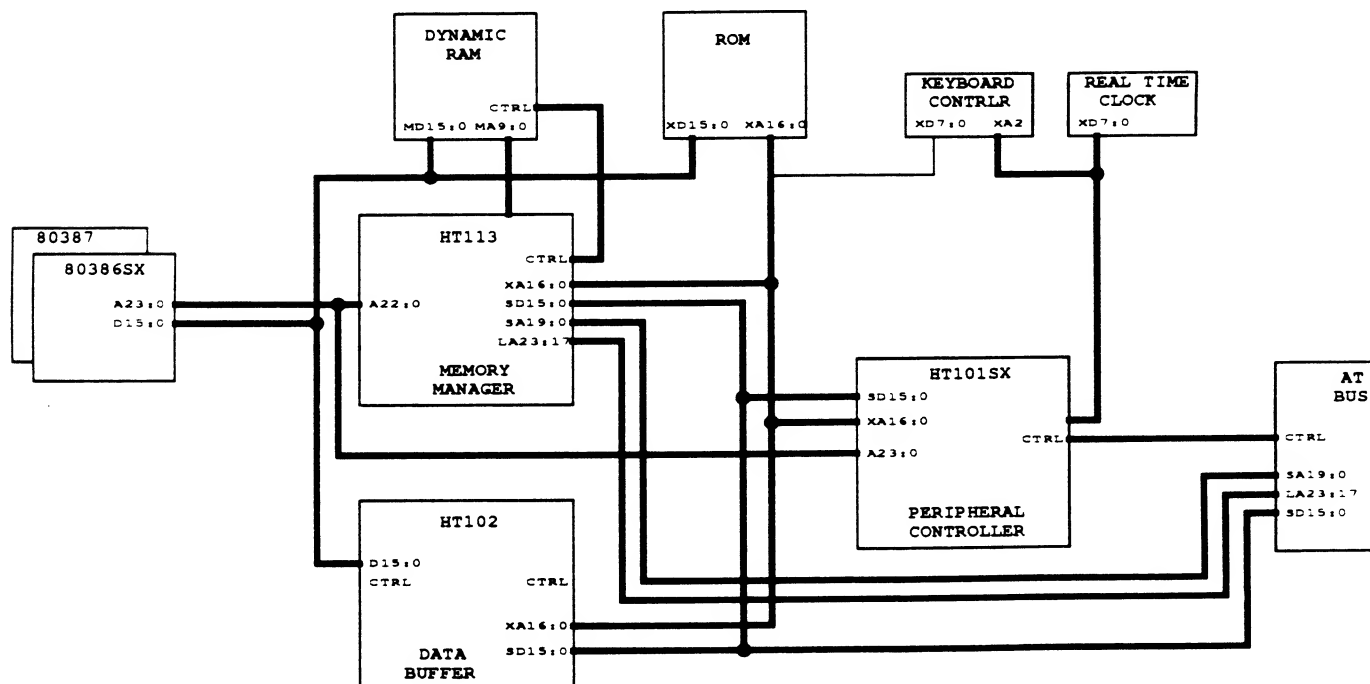
- (1) 82284 compatible clock generator
- (1) 8284 compatible OSC Clock generator
- (2) 8237 compatible DMA Controllers

**Cache:** No

**Clock Speed:** na

**Main Memory Support:** No

- (1) 74612 compatible Memory Mapper
- (1) 8254 compatible Programmable Timer
- (2) 8259 compatible Interrupt Controllers



Headland HTK113SX Chip Set

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** HT102, Data Buffer (part of HTK113SX Chip Set)

**Availability:** ?

**Second Source:** none

**Functions Contained:**

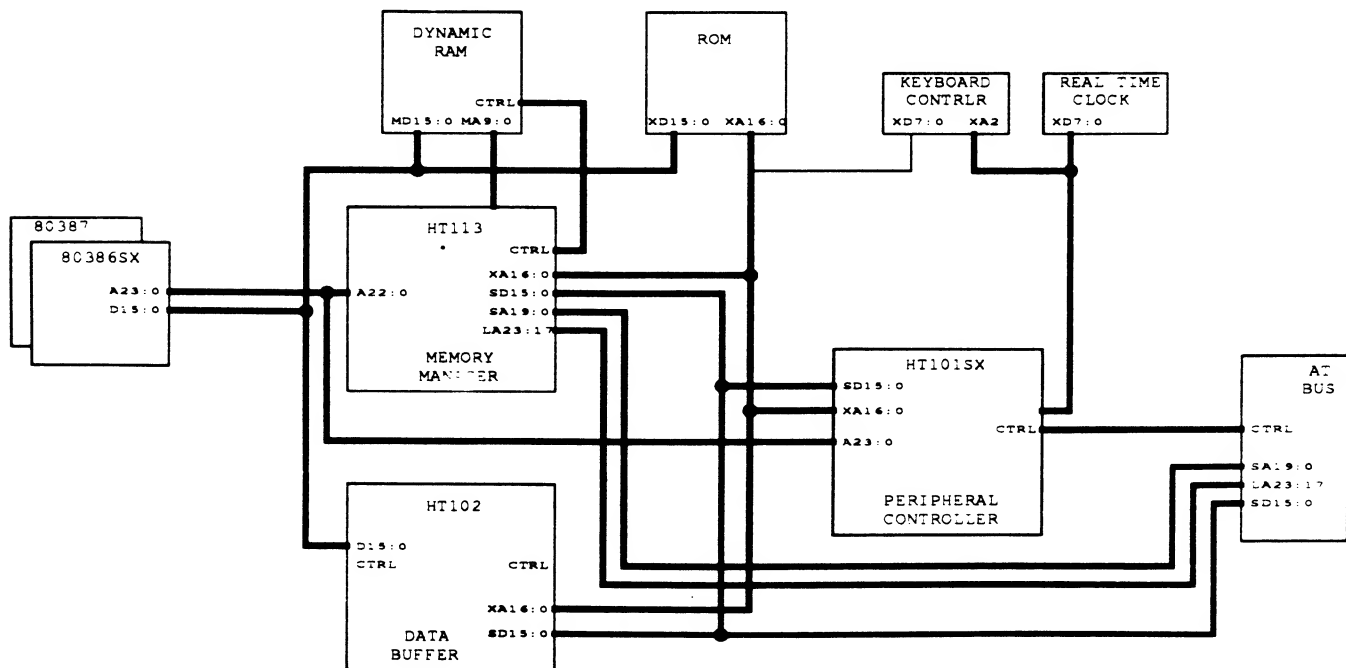
Integrates functions of data transceivers, memory buffers and parity generators/checkers

---

**Cache:** No

**Clock Speed:** na

**Main Memory Support:** No



Headland HTK113SX Chip Set



**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** HT113, Advanced Memory Manager (part of HTK113SX Chip Set)

**Availability:** 1990

**Second Source:** none

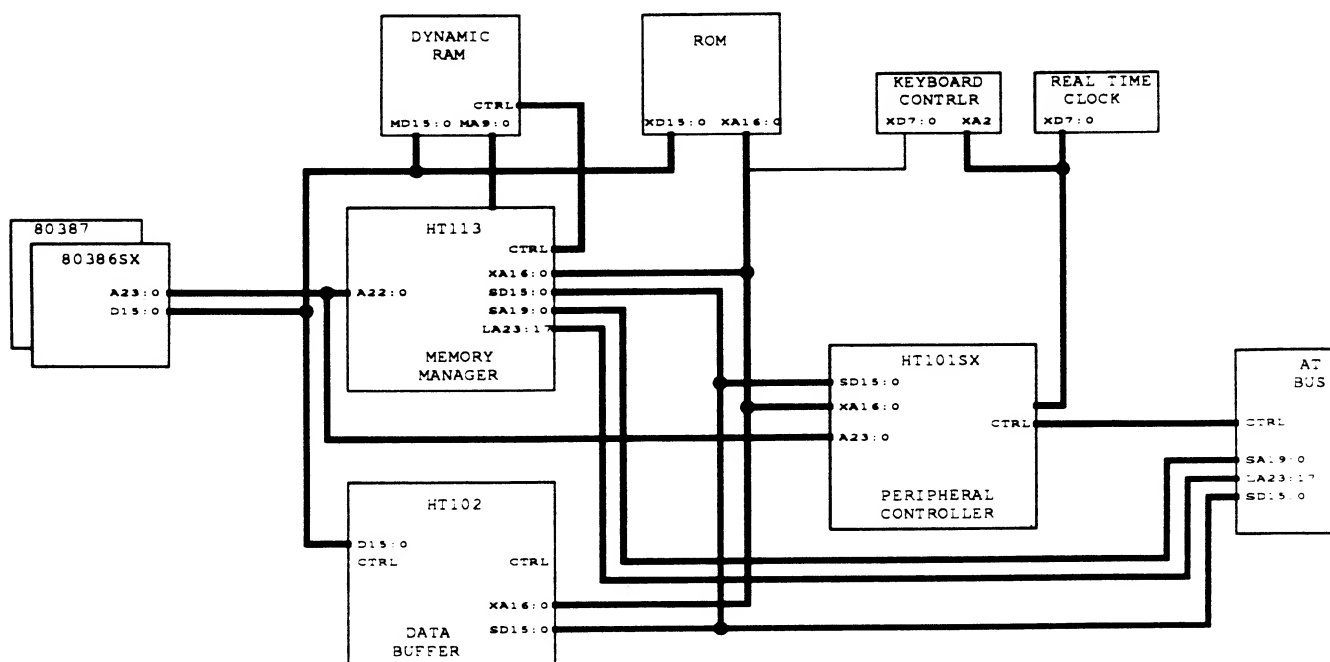
**Functions Contained:**

Supports LIM EMS 4.0 (2 sets of 32 map registers) Utilizes 16K EMS page size

**Cache:** No

**Clock Speed:** na

**Main Memory Support:** Yes



Headland HTK113SX Chip Set

## Personal Computer Design

---

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** HT132, CPU/Memory Controller (part of HTK131 386 Chip Set)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Supports up to 32 MB of DRAM (1 to 4 banks of page interleaved)

Supports 256K or 1M DRAMs

Provides 16- to 8-bit bus conversion

**Cache:** No

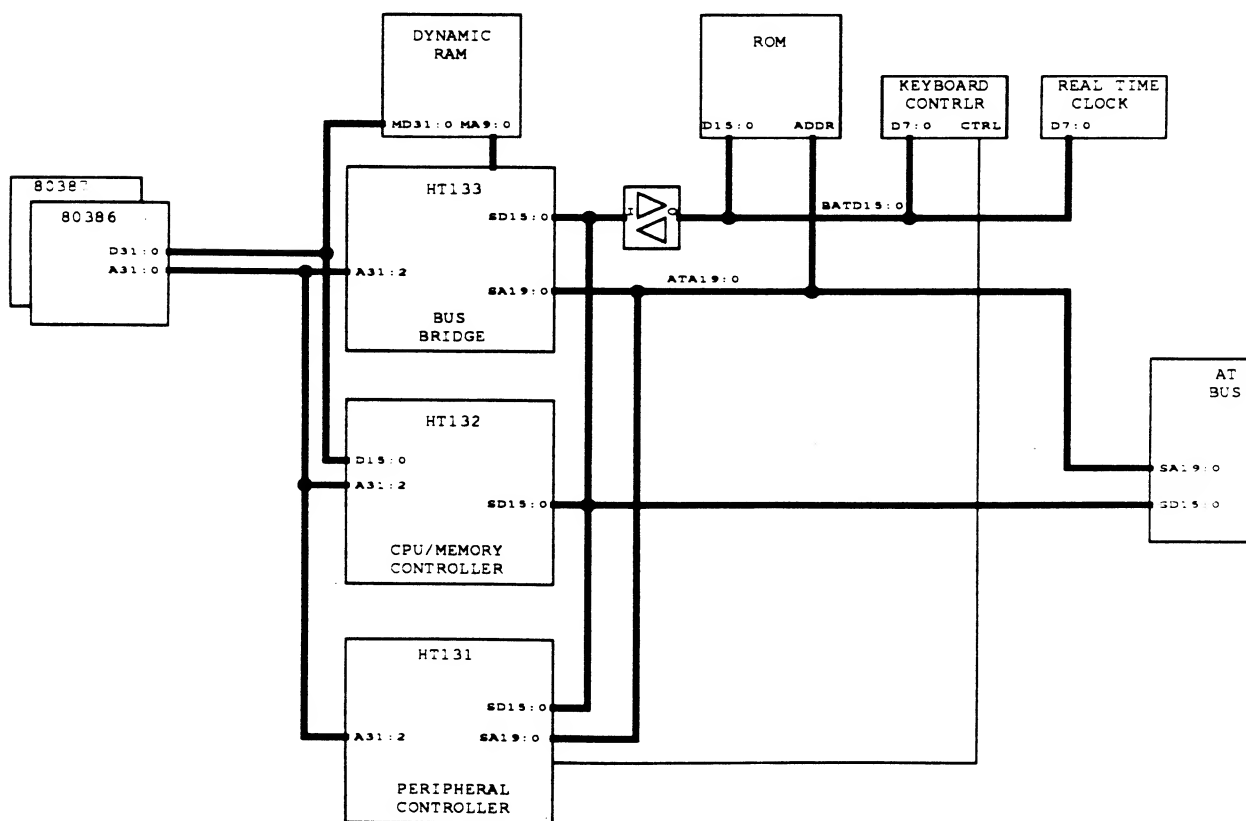
**Clock Speed:** 20, 25, & 33 MHz

**Main Memory Support:** Yes

Supports video and system ROM shadowing

Provides parity generation/checking

---



Headland HTK131 Chip Set

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** HT131, Peripheral Controller (part of HTK131 386 Chip Set)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Provides clock dividers for slow- and fast-speed mode

Peripheral interface to (2) Serial and (1) parallel port

Provides video configuration register shadow

(1) 82284 compatible clock generator

(1) 8284 compatible OSC Clock generator

(2) 8237 compatible DMA Controllers

**Cache:** No

**Clock Speed:** 20, 25, & 33 MHz

**Main Memory Support:** No

Provides DMA and refresh wait states

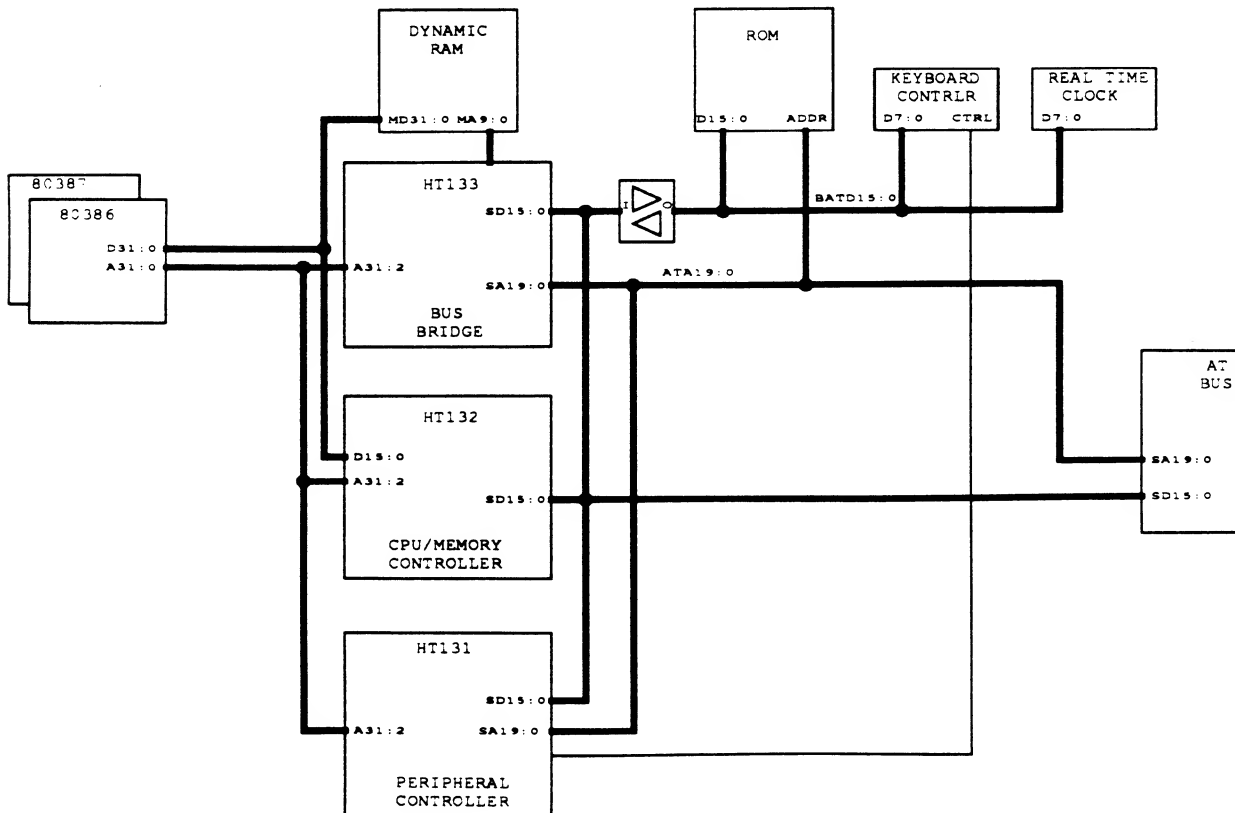
Supports port 92h, fast reset and fast A20GATE

Provides additional refresh wait states

(1) 74612 compatible Memory Mapper

(1) 8254 compatible Programmable Timer

(2) 8259 compatible Interrupt Controllers



Headland HTK131 Chip Set

## Personal Computer Design

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** HT133, Bus Bridge Interface (part of HTK131 386 Chip Set)

**Availability:** 1989

**Second Source:** none

**Functions Contained:**

Slave to HT132

Provides a bridge between 32-bit CPU data and 16-bit AT-compatible bus

Provides Address latch and Memory address multiplexer

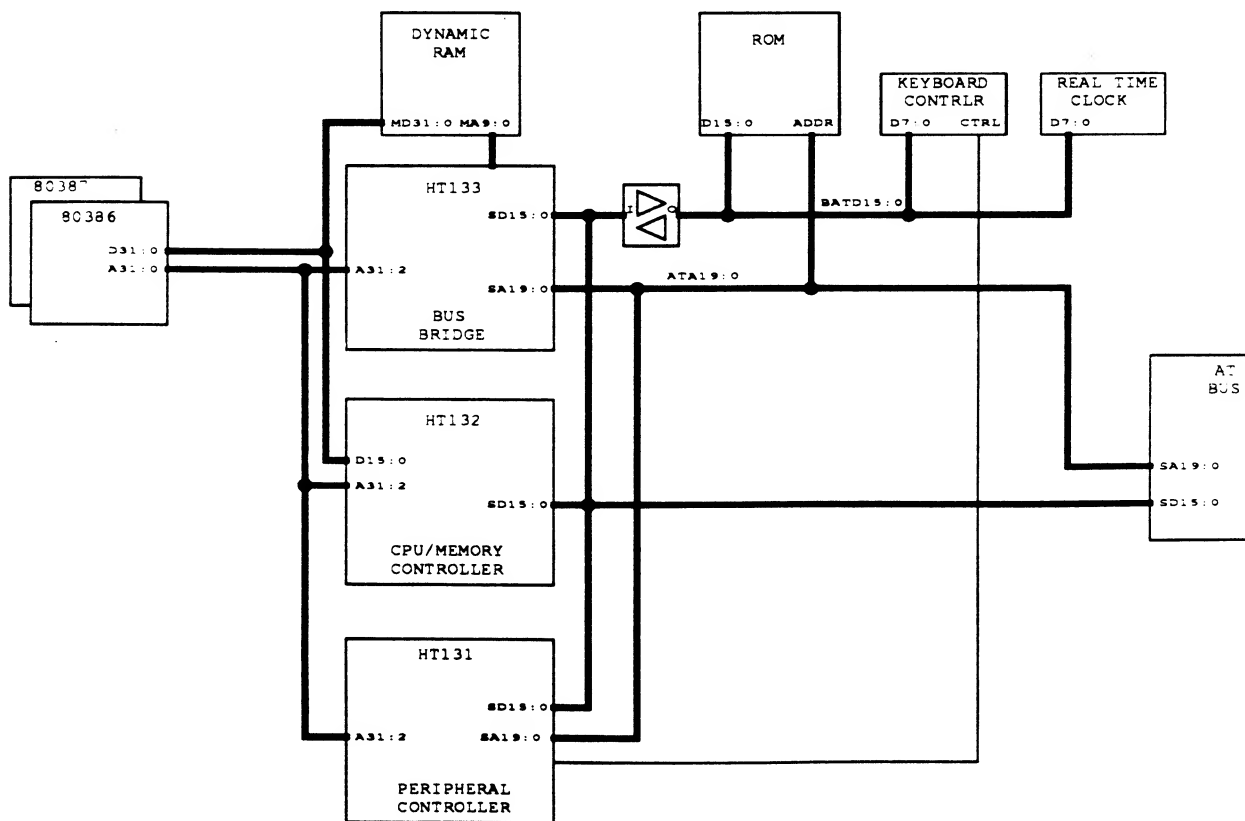
Page mode violation detection

PBEN and low order ATA generation

**Cache:** No

**Clock Speed:** 20, 25, & 33 MHz

**Main Memory Support:** Yes



Headland HTK131 Chip Set

**Manufacturer:** Headland Technology Inc.

**Processor Supported:** 80486

**System Bus:** AT

**Part:** HT135, CPU Interface (part of HTK135 486 Chip Set)

**Availability:** 1989

**Second Source:** none

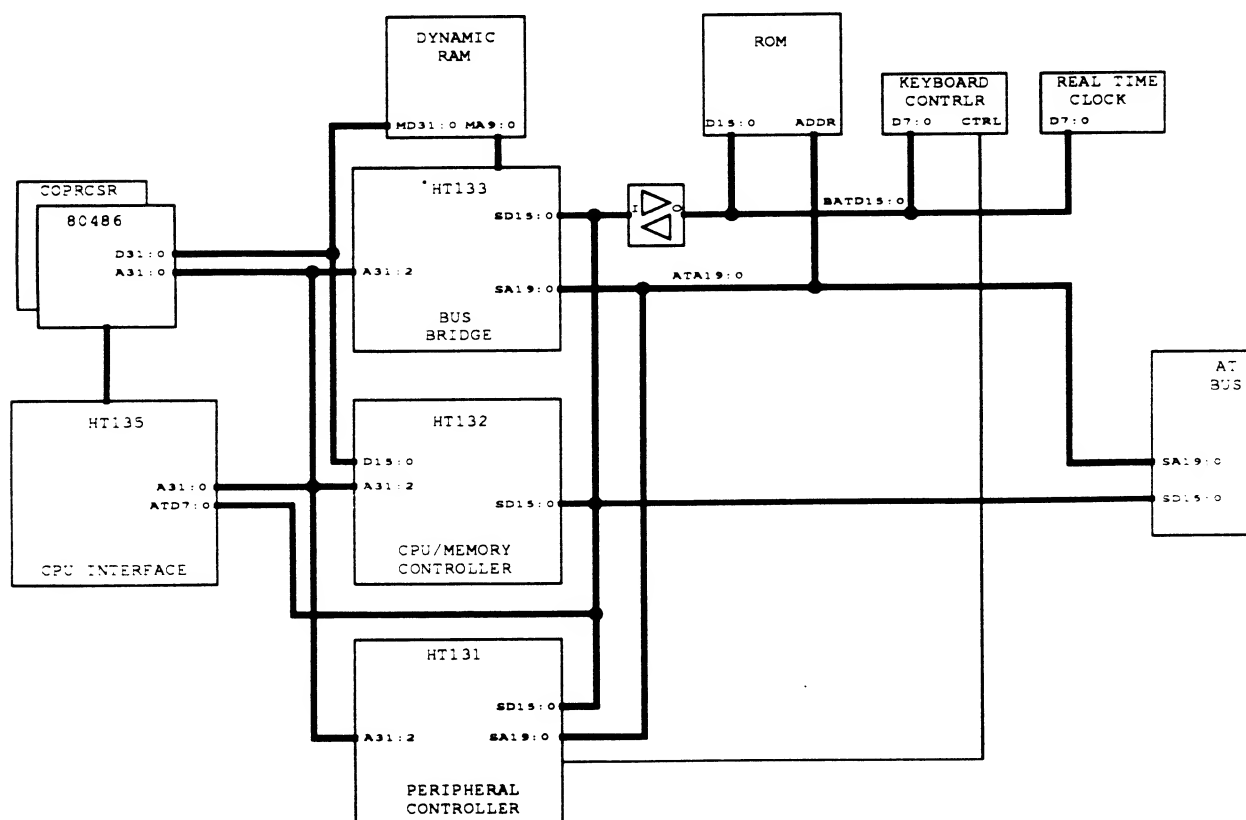
**Functions Contained:**

?

**Cache:** No

**Clock Speed:** 20, 25, & 33 MHz

**Main Memory Support:** No



Headland HTK135 486 Chip Set

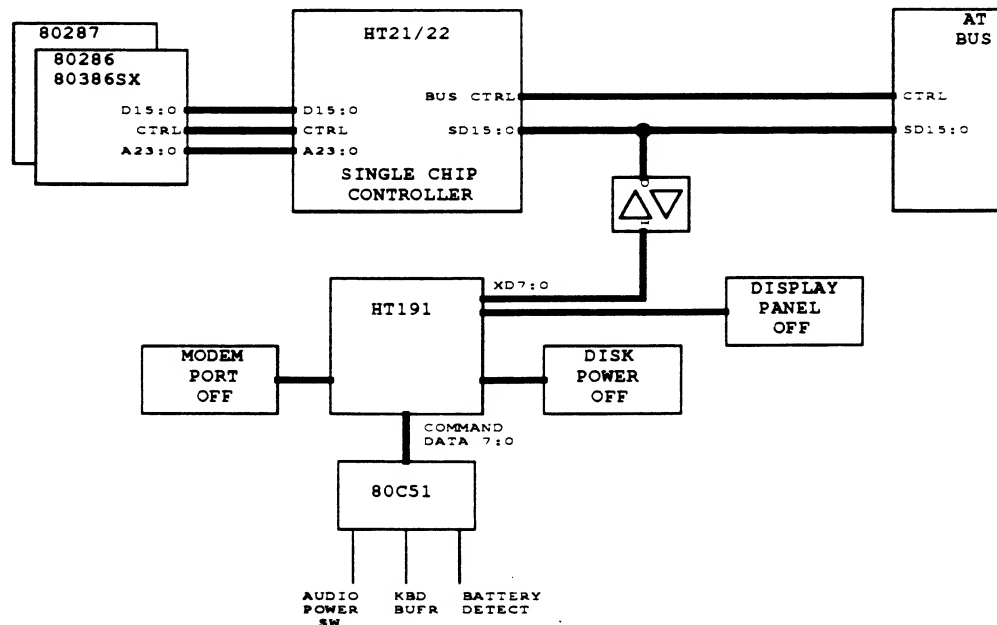
## Personal Computer Design

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**Manufacturer:** Headland Technology Inc.  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT  
**Part:** HT191, Power Management Single Chip  
**Availability:** 1990  
**Second Source:** none  
**Functions Contained:**  
Fully programmable power management chip  
Supports suspend/resume, standby & sleep modes  
Monitors peripheral activity and battery level  
80C51 power management firmware available

**Cache:** No  
**Clock Speed:** na  
**Main Memory Support:** No

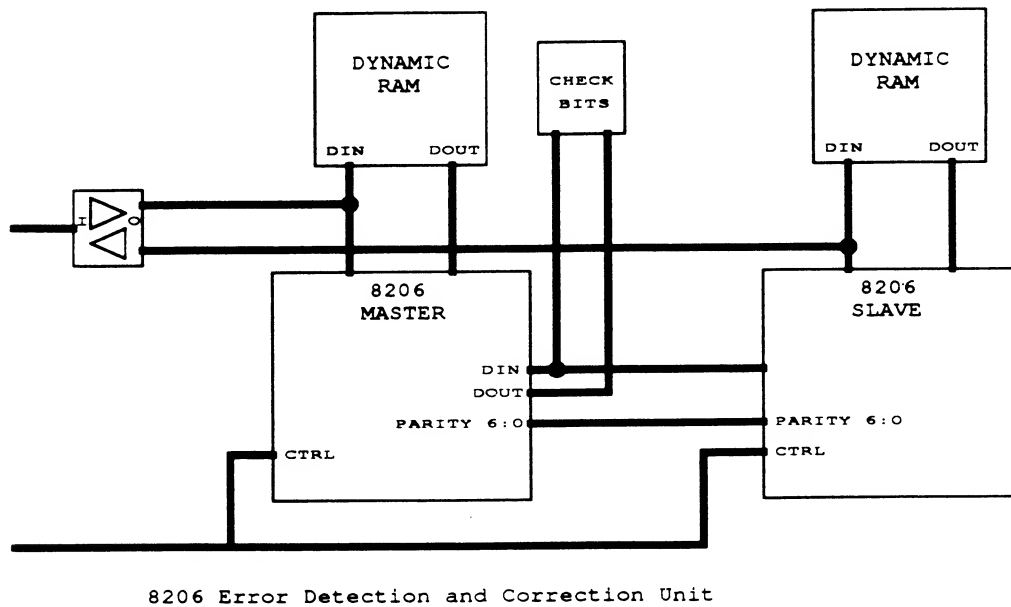
Programmable hardware decodes for I/O devices  
User programmable event timer  
Programmable chip selects (x4)  
Support device to interface AT bus with 8051



Headland HT191 Power Management Single Chip

**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386, 80286  
**System Bus:** AT  
**Part:** 8206 Error Detection and Correction Unit  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
 Separate I/O busses  
 Supports read with/without correction, writes, read-modify-writes  
 Supports automatic error scrubbing

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** No



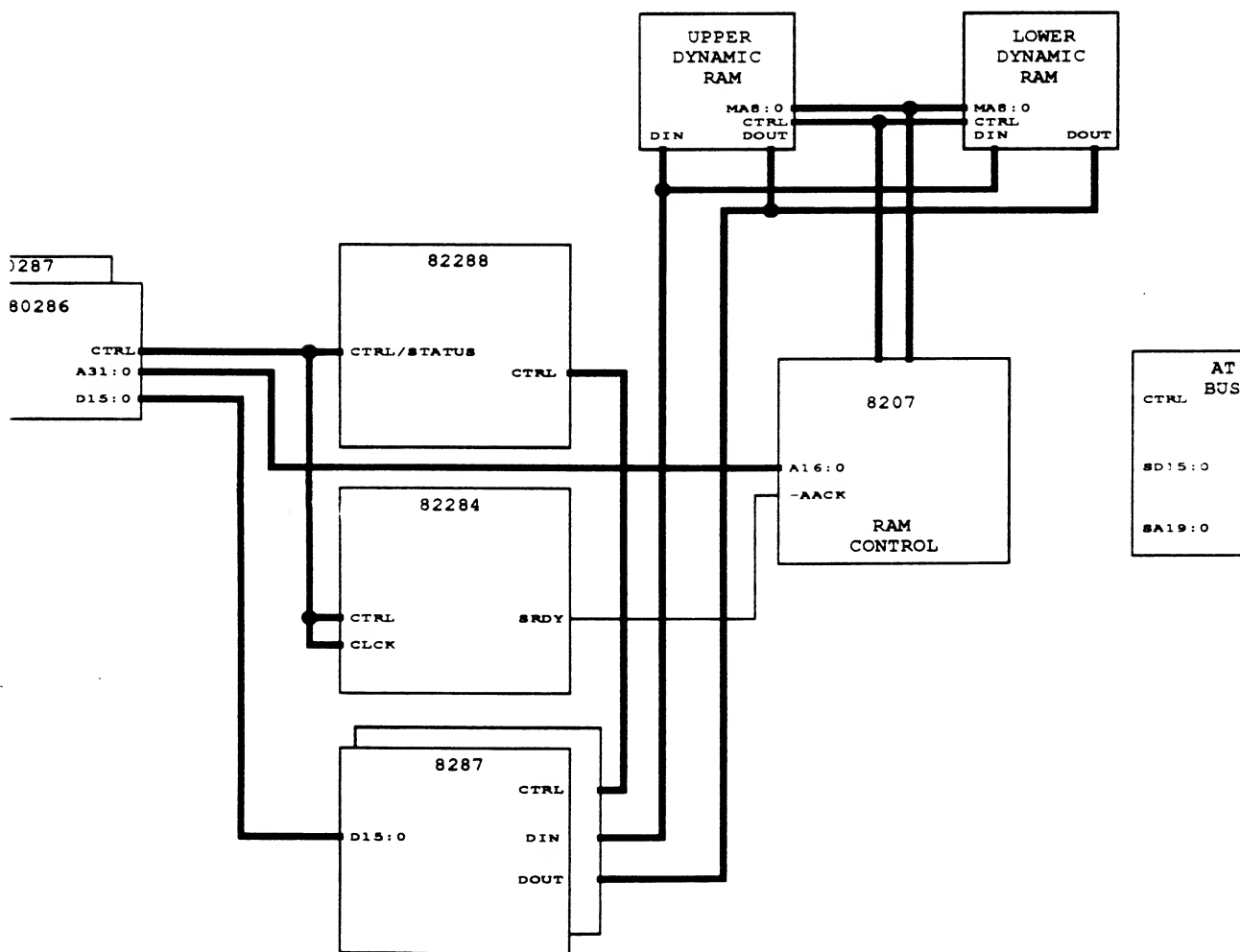
## Personal Computer Design

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**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386, 80286  
**System Bus:** AT  
**Part:** 8207 Dual-Port Dynamic RAM controller  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
4 programmable refresh modes  
Provides Auto RAM initialize  
Supports transparent Memory Scrubbing  
Supports Async/Sync on either port  
Provides signals to control the 8206

---

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** Yes, 2 MB

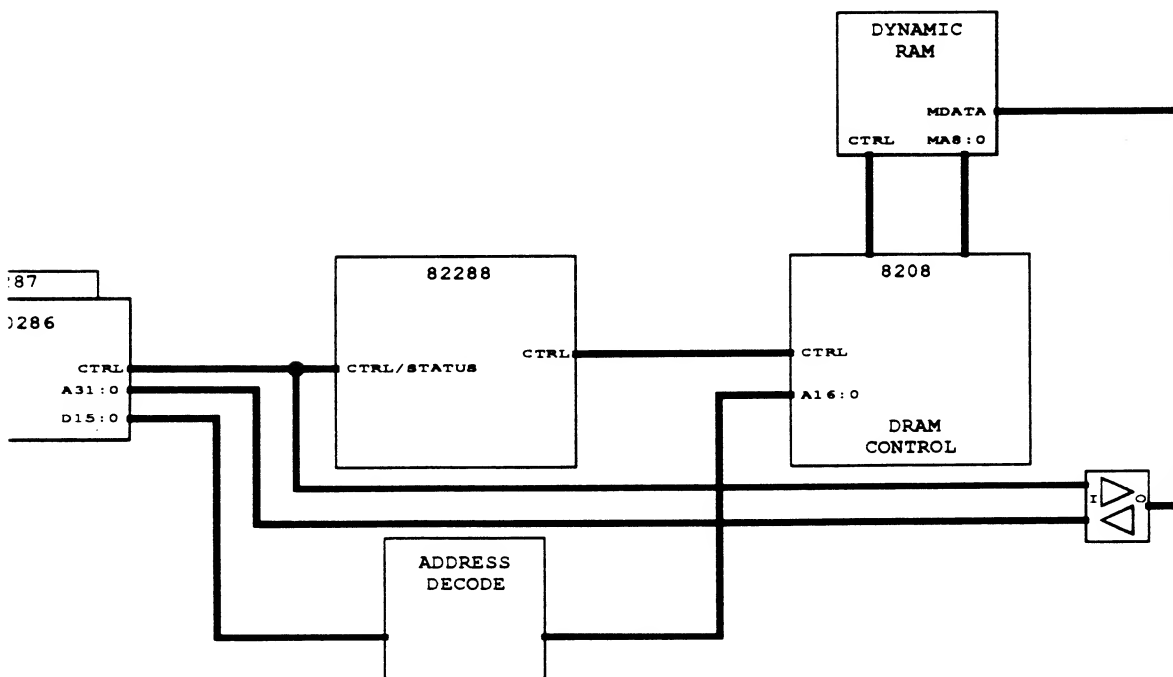


8207 Dual Port DRAM Control



**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386  
**System Bus:** AT  
**Part:** 82C08 CHMOS Dynamic RAM Controller  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
 Zero wait state  
 Power down mode with programmable memory refresh  
 5 refresh modes  
 Auto RAM warm-up

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** Yes, 1 MB



8208 CHMOS DRAM Control

## Personal Computer Design

---

**Manufacturer:** Intel

**Processor Supported:** 80486, 80386, 80286, 8086

**System Bus:** AT

**Part:** 8231A Arithmetic Processing Unit

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

Fixed point single/double 32-bit precision

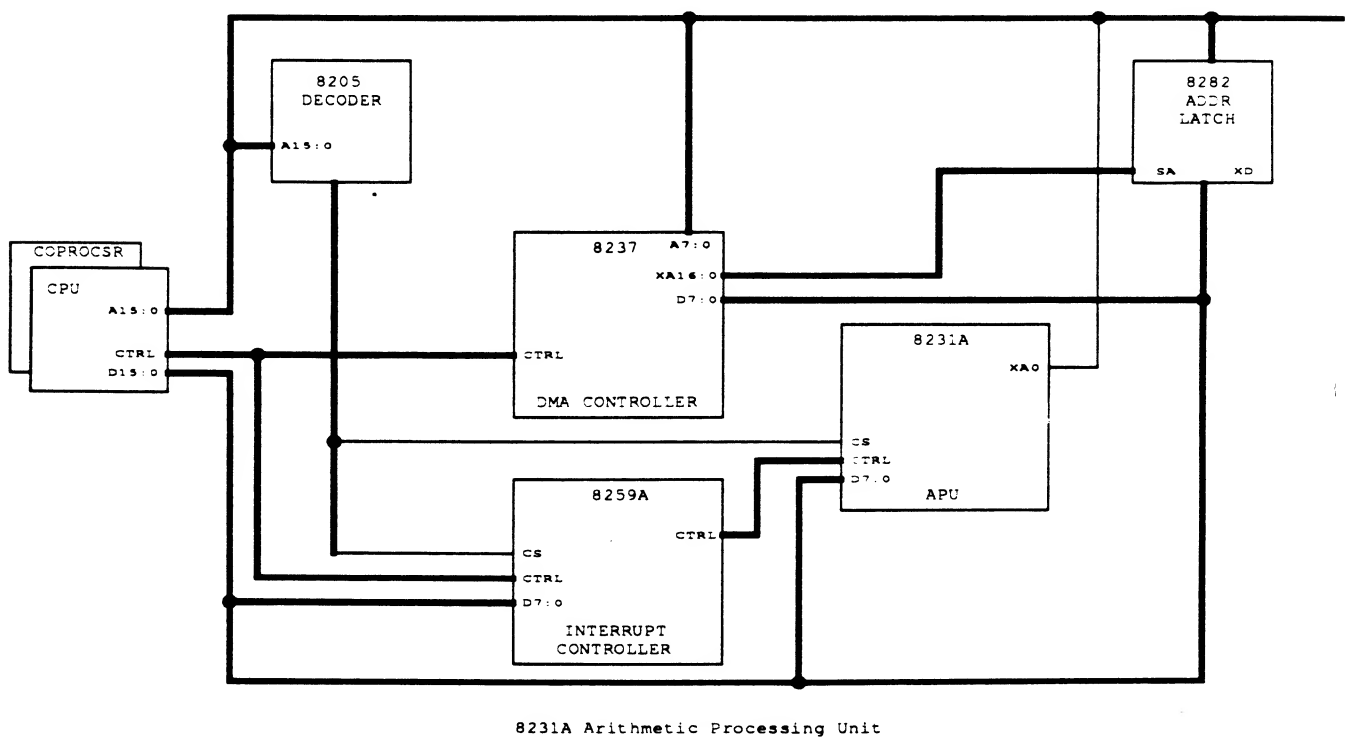
Floating point double 32-bit precision

---

**Cache Memory:** No

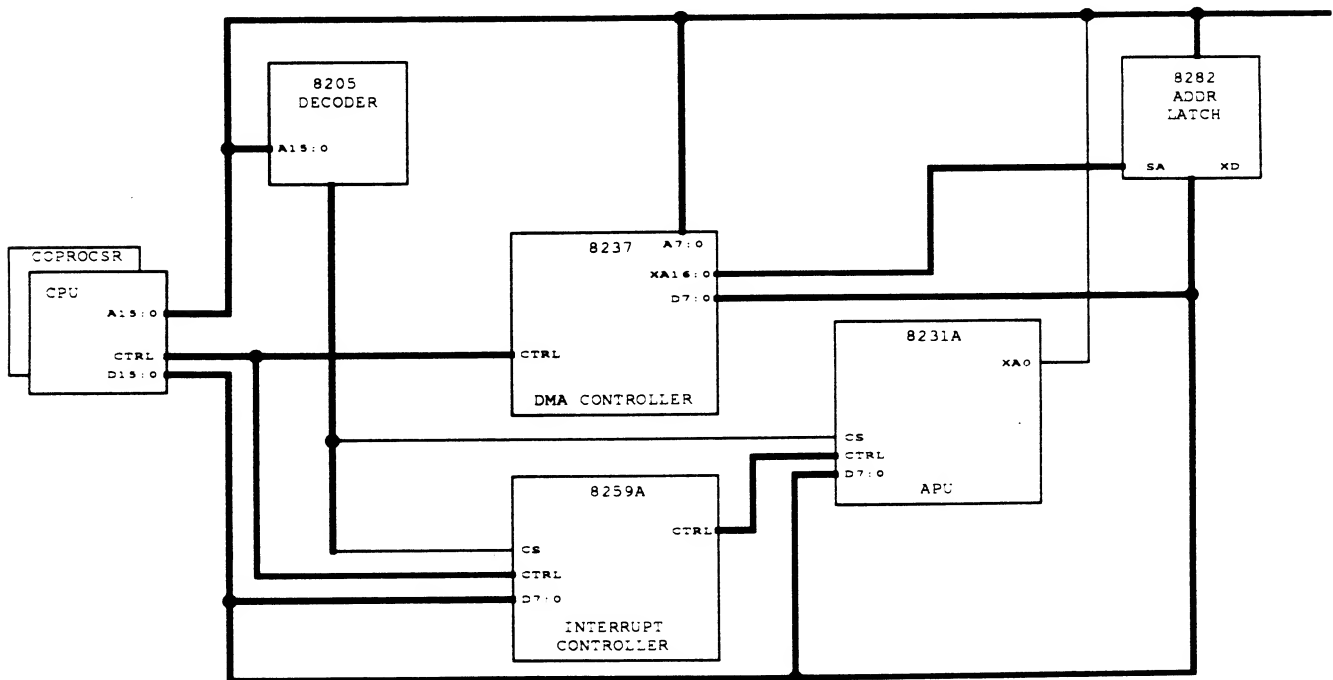
**Clock Speed:** NA

**Main Memory Support:** Yes



**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386  
**System Bus:** AT  
**Part:** 8237A programmable DMA controller  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
 4 independent DMA channels  
 Expandable to any number of channels  
 Software DMA requests  
 Auto-initialize all channels

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** Yes



8231A Arithmetic Processing Unit

## **Personal Computer Design**

---

**Manufacturer:** Intel

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 80C51SL Low Power Keyboard Controller

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

Provides keyboard scan

Supports expanded memory

Provides power management

---

**Cache Memory:** No

**Clock Speed:** NA

**Main Memory Support:** No

Schematic Not Available At Press Time

**Manufacturer:** Intel

**Processor Supported:** PS/2, 80386

**System Bus:** PS/2

**Part:** 82077 floppy disk controller (part of 82311 Chip set)

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

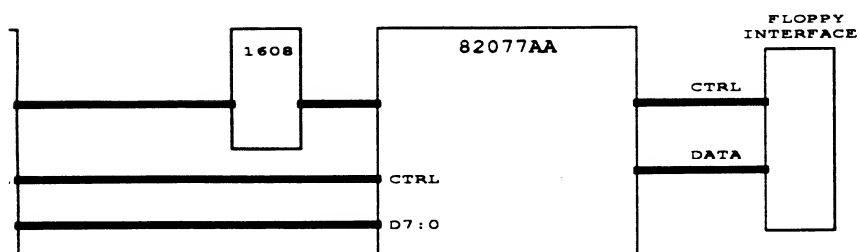
Supports 3.5, 5.25 inch drives, and 4 MB drives

---

**Cache Memory:** No

**Clock Speed:** 16, 20, 25 Mhz

**Main Memory Support:** No



Intel 82077AA Floppy Disk Controller

## **Personal Computer Design**

---

**Manufacturer:** Intel  
**Processor Supported:** 80386  
**System Bus:** AT  
**Part:** 82077SL floppy disk controller  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
Supports 3.5, 5.25 inch drives, and 4 MB drives  
Supports auto power-down

---

**Cache Memory:** No  
**Clock Speed:** 16, 20, 25 Mhz  
**Main Memory Support:** No

Schematic Not Available At Press Time

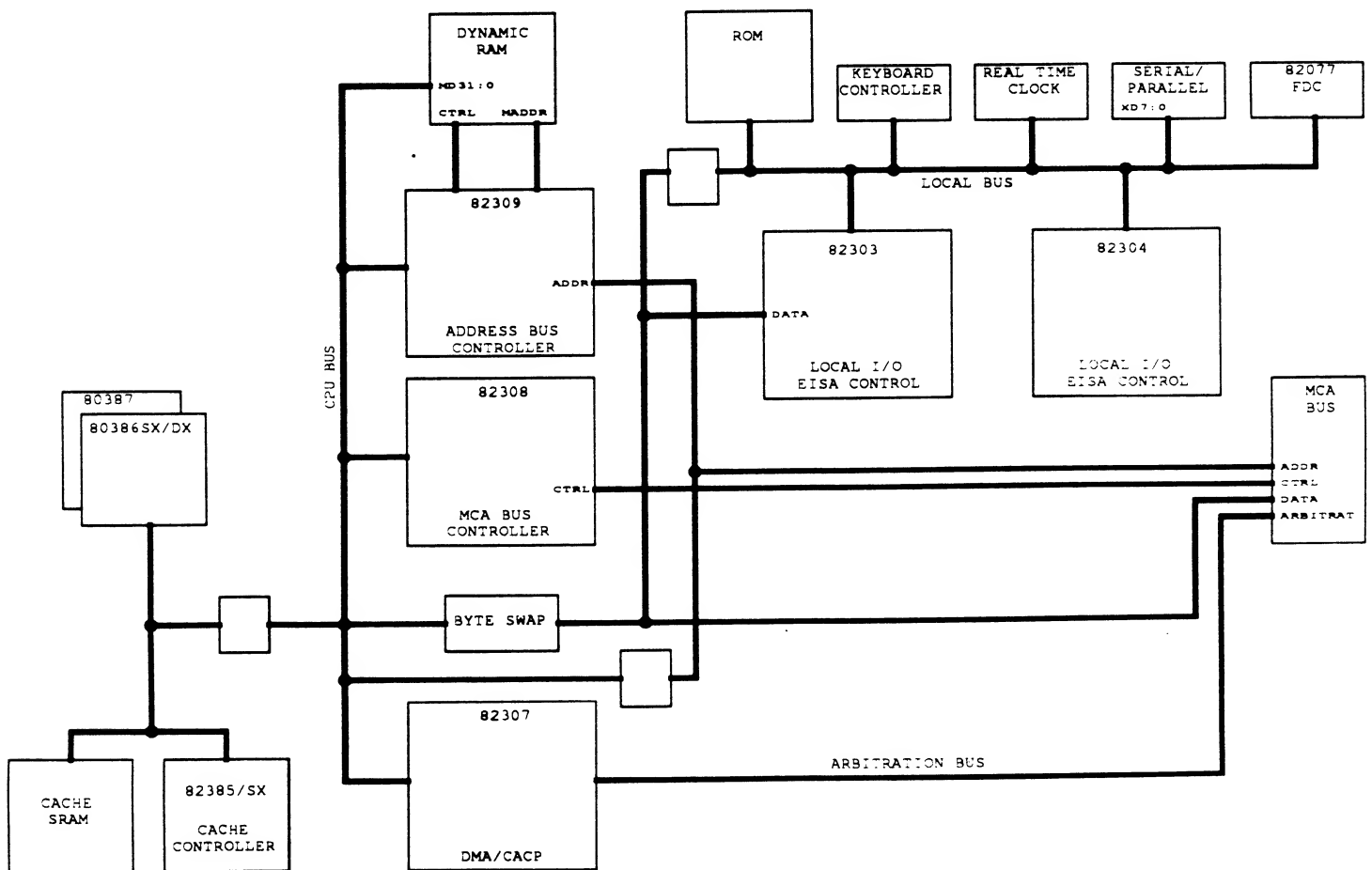
**Manufacturer:** Intel  
**Processor Supported:** PS/2, 80386  
**System Bus:** PS/2  
**Part:** 82303 Local Channel Support Chip (part of 82311 Chip set)  
**Availability:** NA

**Cache Memory:** No  
**Clock Speed:** 16, 20, 25 Mhz  
**Main Memory Support:** No

**Second Source:** NA

**Functions Contained:**

Logic for parallel or bidirectional ports  
 Card setup port (96H)  
 Peripheral bus-address latches  
 Provides signals to support system setup functions



Intel 82311 MCA Peripheral Chipset

## Personal Computer Design

**Manufacturer:** Intel

**Processor Supported:** PS/2, 80386

**System Bus:** PS/2

**Part:** 82304 Local Channel Support Chip (part of 82311 Chip set)

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

Supports local bus I/O peripheral components

VGA controller

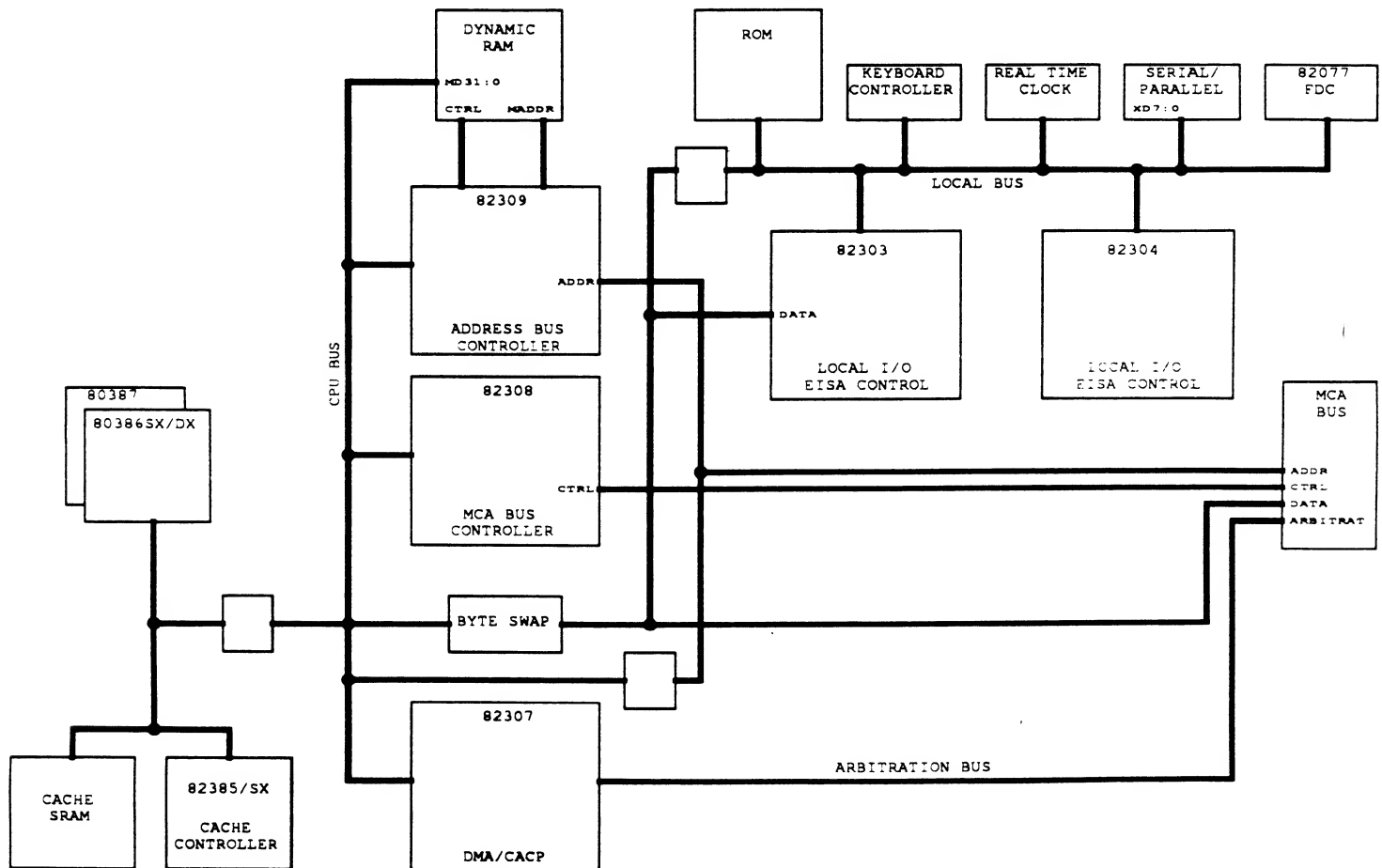
Contains 3 programmable timers/counters

(2) programmable interrupt controllers

**Cache Memory:** No

**Clock Speed:** 16, 20, 25 Mhz

**Main Memory Support:** No



Intel 82311 MCA Peripheral Chipset



**Manufacturer:** Intel

**Processor Supported:** PS/2, 80386

**System Bus:** PS/2

**Part:** 82307 DMA/CACP controller (part of 82311 Chip set)

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

DMA functions

Supports 8-bit & 16-bit transfers

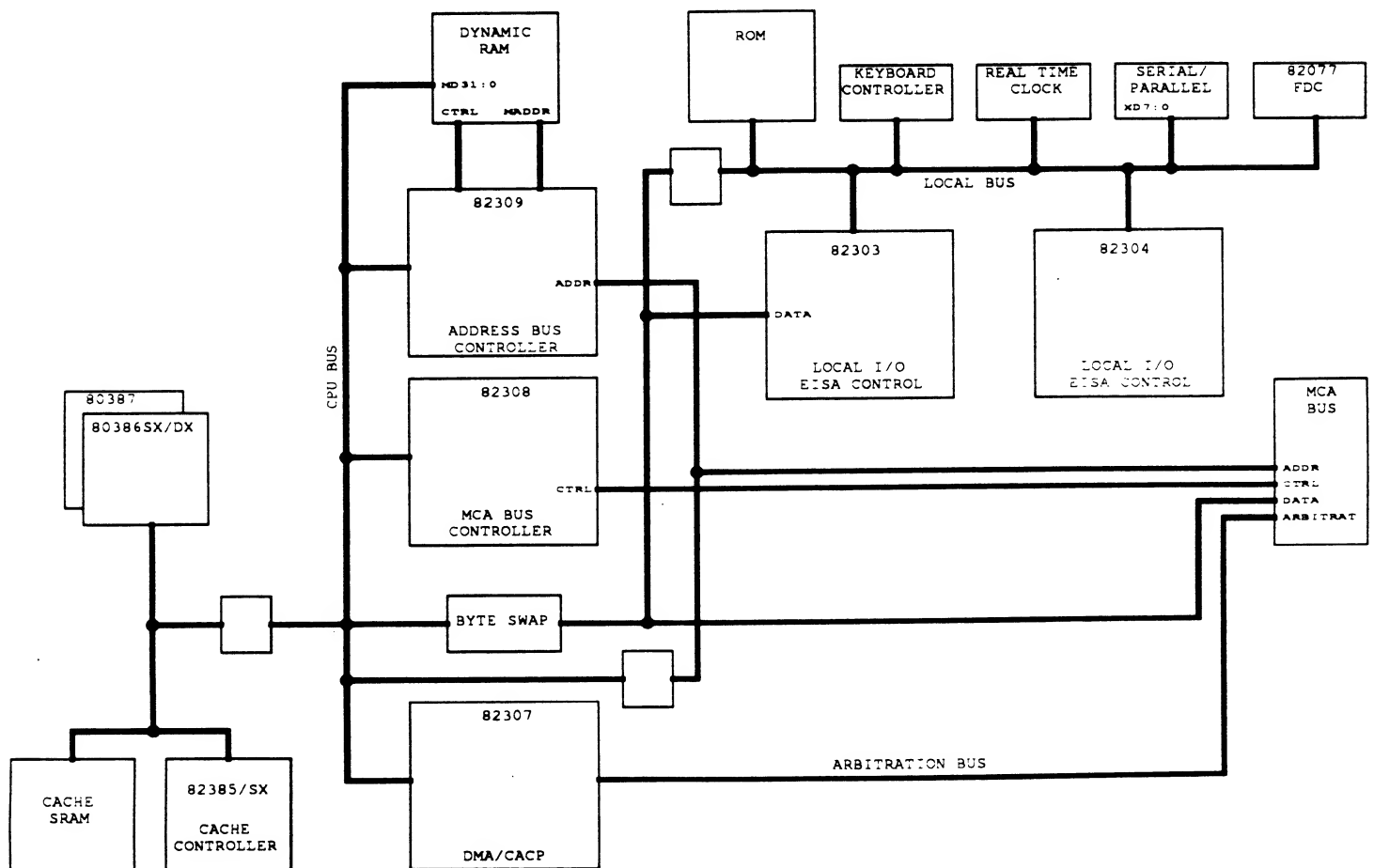
Supports math co-processors

Refresh-address generation and cycling

**Cache Memory:** No

**Clock Speed:** 16, 20, 25 Mhz

**Main Memory Support:** Yes



Intel 82311 MCA Peripheral Chipset

## Personal Computer Design

**Manufacturer:** Intel

**Processor Supported:** PS/2, 80386

**System Bus:** PS/2

**Part:** 82308 Micro Channel Bus Controller (part of 82311 Chip set)

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

Generates timing signals that control data transfers between the CPU, DMA, memory and the Micro Channel bus

Supports slow I/O devices

External byte-swap logic

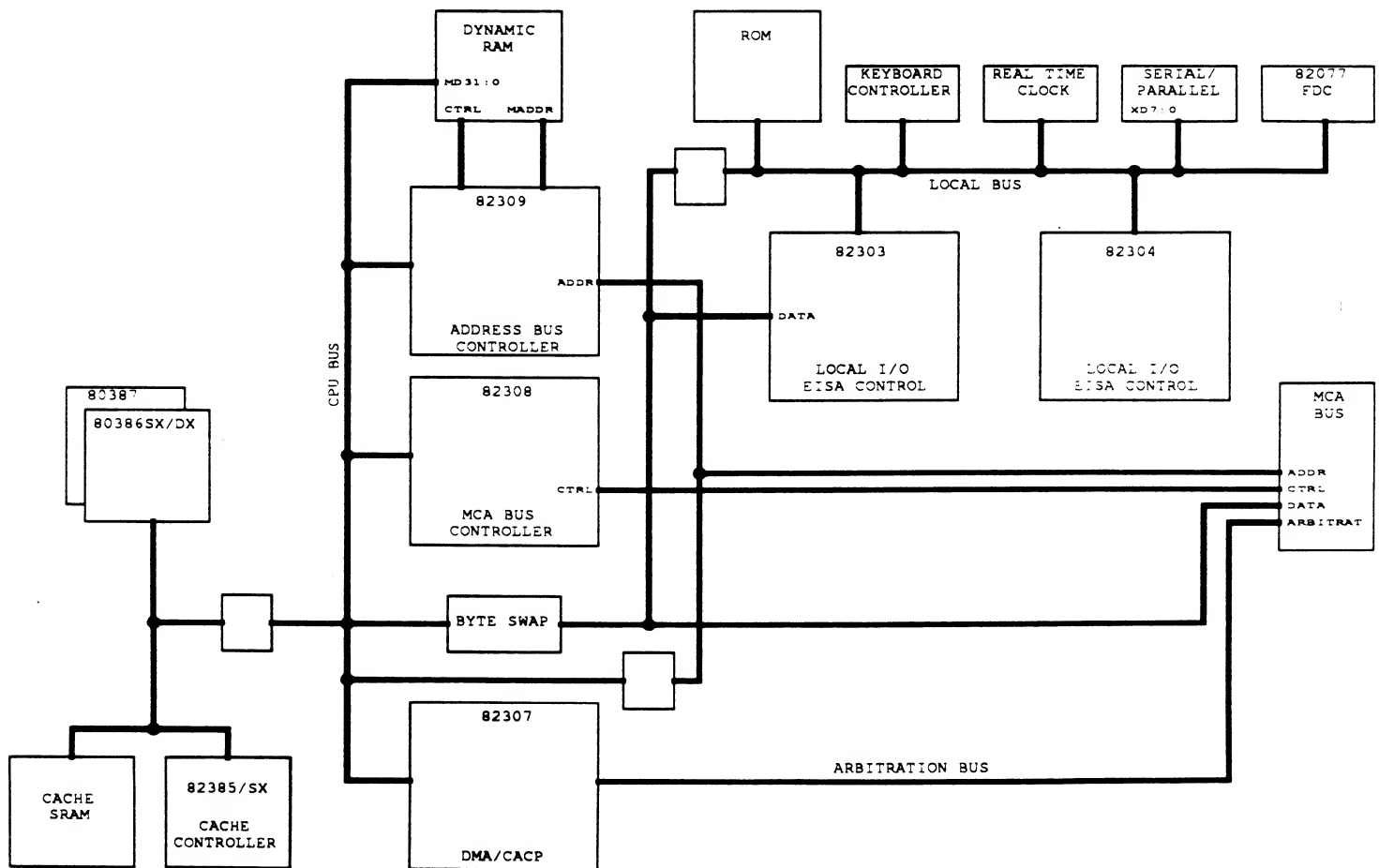
Parity check

CPU read/reset condition

**Cache Memory:** No

**Clock Speed:** 16, 20, 25 Mhz

**Main Memory Support:** Yes



Intel 82311 MCA Peripheral Chipset

**Manufacturer:** Intel

**Processor Supported:** PS/2, 80386

**System Bus:** PS/2

**Part:** 82309 address-bus controller (part of 82311 Chip set)

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

Supports a variety of DMA configurations

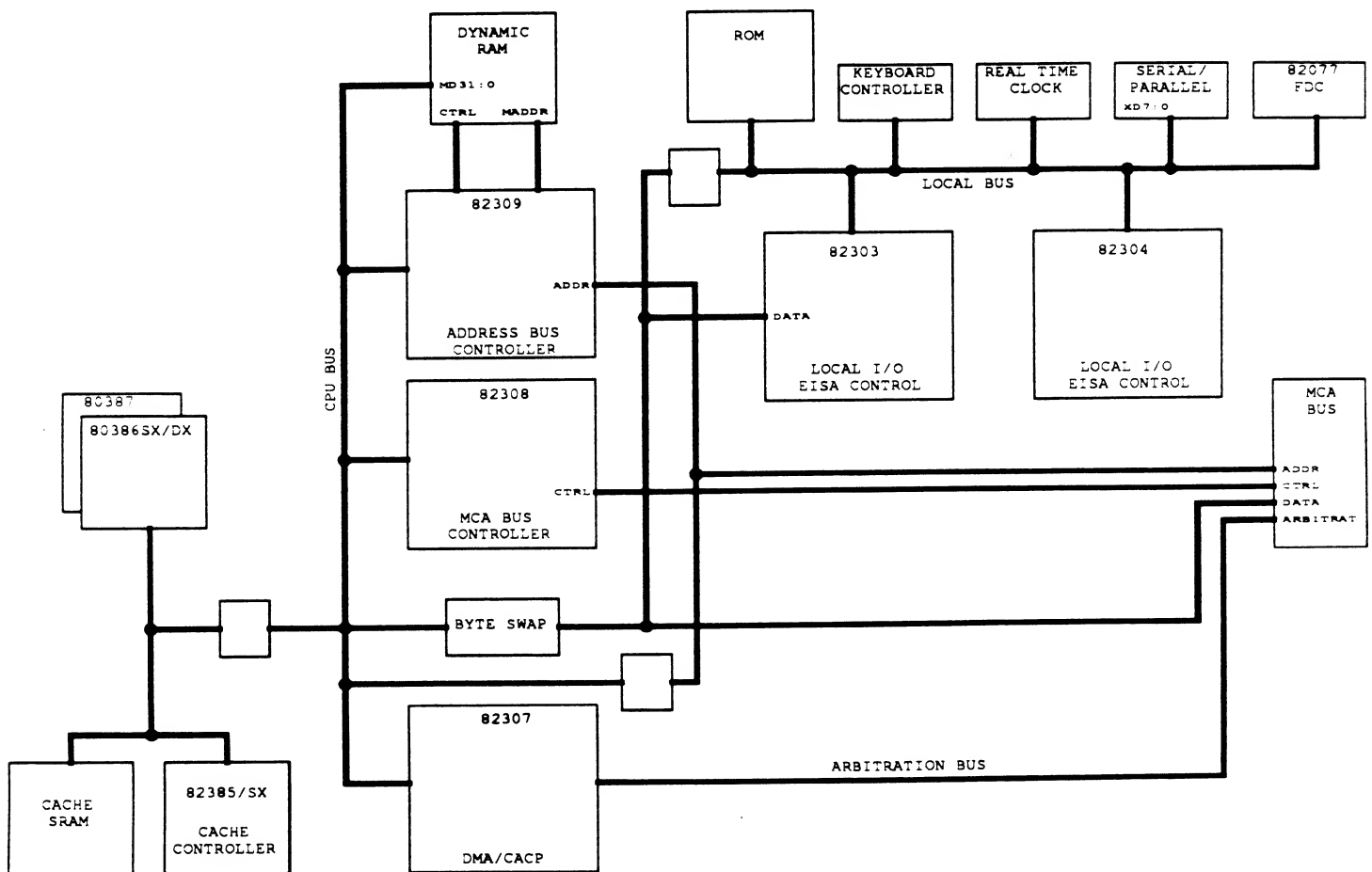
Supports 256 KB, 1 MB and 4 MB DRAMS

Supports 16 MB address mapping, RAS/CAS generation, address multiplexing, and refresh timing

**Cache Memory:** No

**Clock Speed:** 16, 20, 25 Mhz

**Main Memory Support:** Yes



Intel 82311 MCA Peripheral Chipset

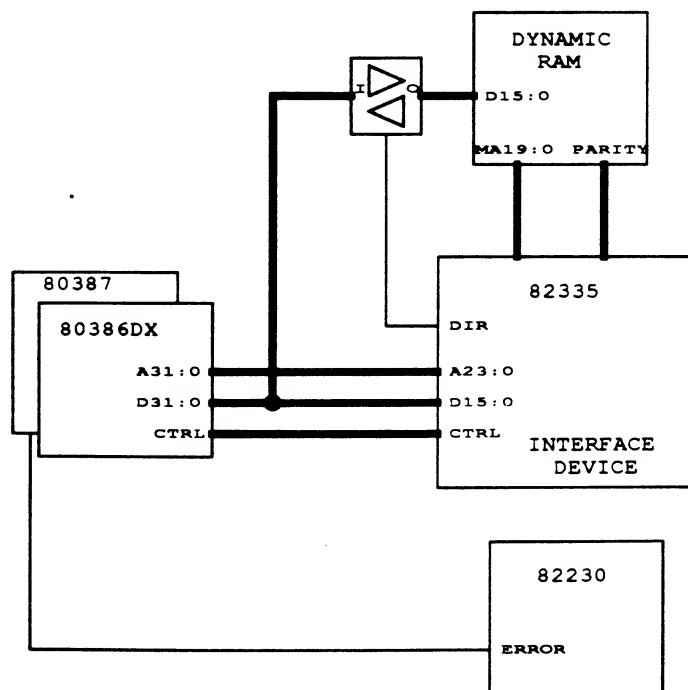
## Personal Computer Design

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**Manufacturer:** Intel  
**Processor Supported:** 80386  
**System Bus:** AT  
**Part:** 82335, High Integration Interface Device  
**Availability:** 1988  
**Second Source:** NA  
**Functions Contained:**  
Page mode/interleaved DRAM support (up to 8 MB)  
Supports shadow RAM  
Parity generation and checking  
80387 synchronous interface

---

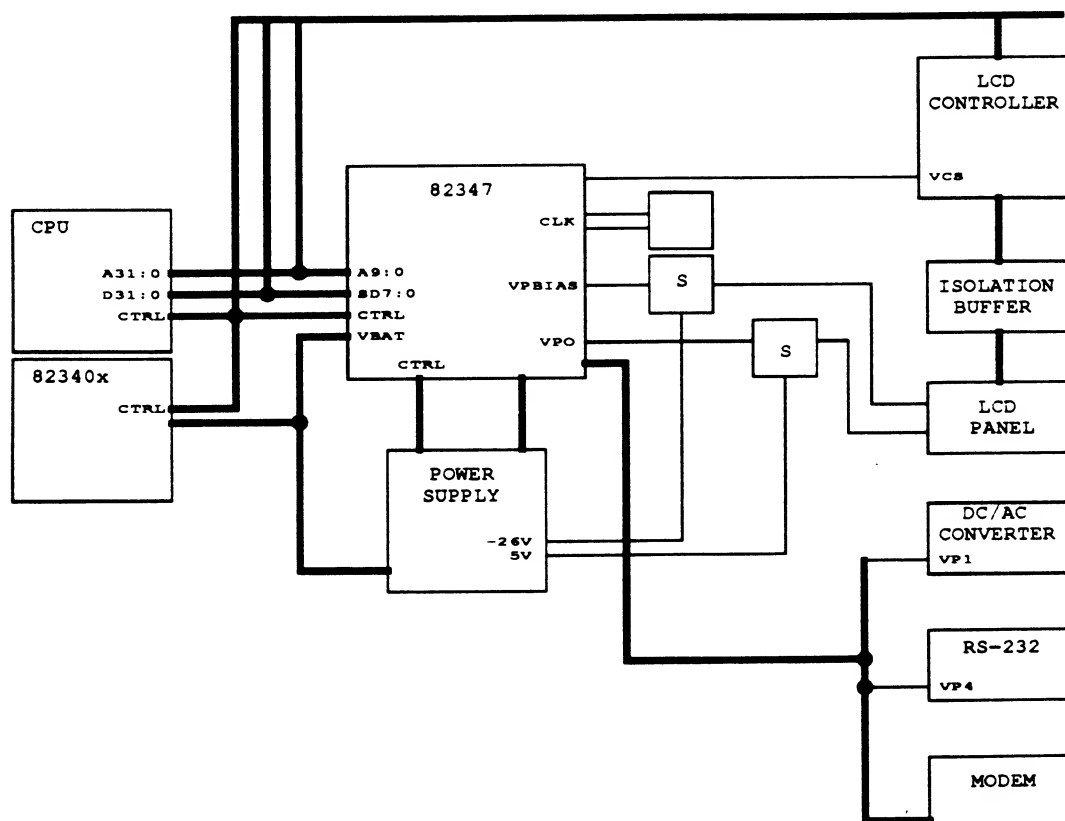
**Cache Memory:** No  
**Clock Speed:** 16 MHz  
**Main Memory Support:** Yes



Intel High-Integration Interface Device

**Manufacturer:** Intel  
**Processor Supported:** 80386  
**System Bus:** AT  
**Part:** 82347 Power Management PC Peripheral  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
 Provides sleep, standby and suspend functions programmable through BIOS  
 Outputs clock to system

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** No

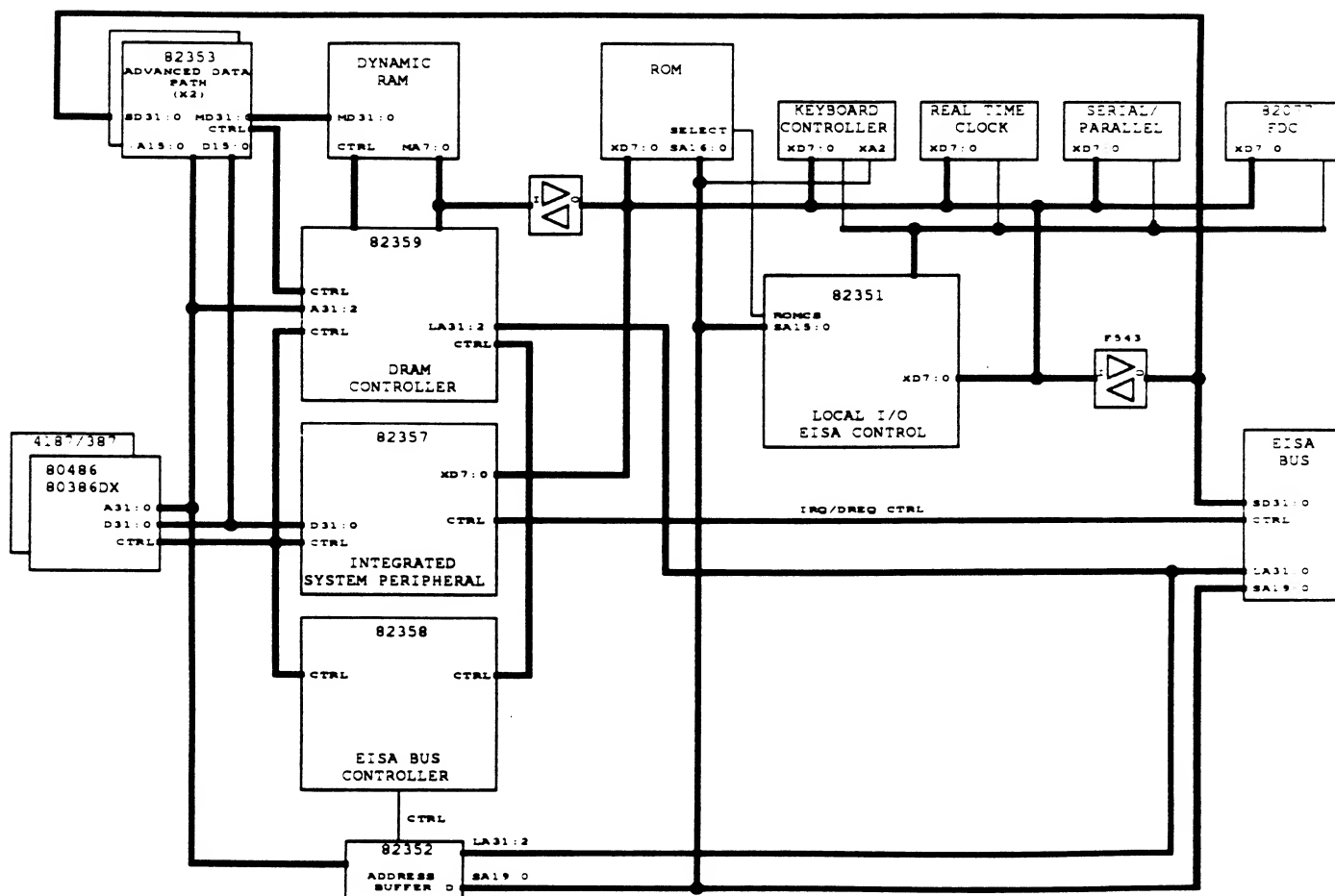


Intel 82347 Power Management PC Peripheral

## Personal Computer Design

**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386  
**System Bus:** EISA/ISA  
**Part:** 82350 EISA Chip Set  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
8, 16, 32-bit DMA cycles  
Non-maskable interrupt logic for multiple NMI control  
Refresh address generation  
Multiple floppy drive controller  
Keyboard & mouse controller

**Cache Memory:** No  
**Clock Speed:** 25, 33 Mhz  
**Main Memory Support:** Yes, 256 MB



Intel 82350 EISA Chipset for the 80486

**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386  
**System Bus:** EISA/ISA  
**Part:** 82351 Local I/O Controller

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** No

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

Address decode and command logic support for 2 serial I/O ports

Parallel port

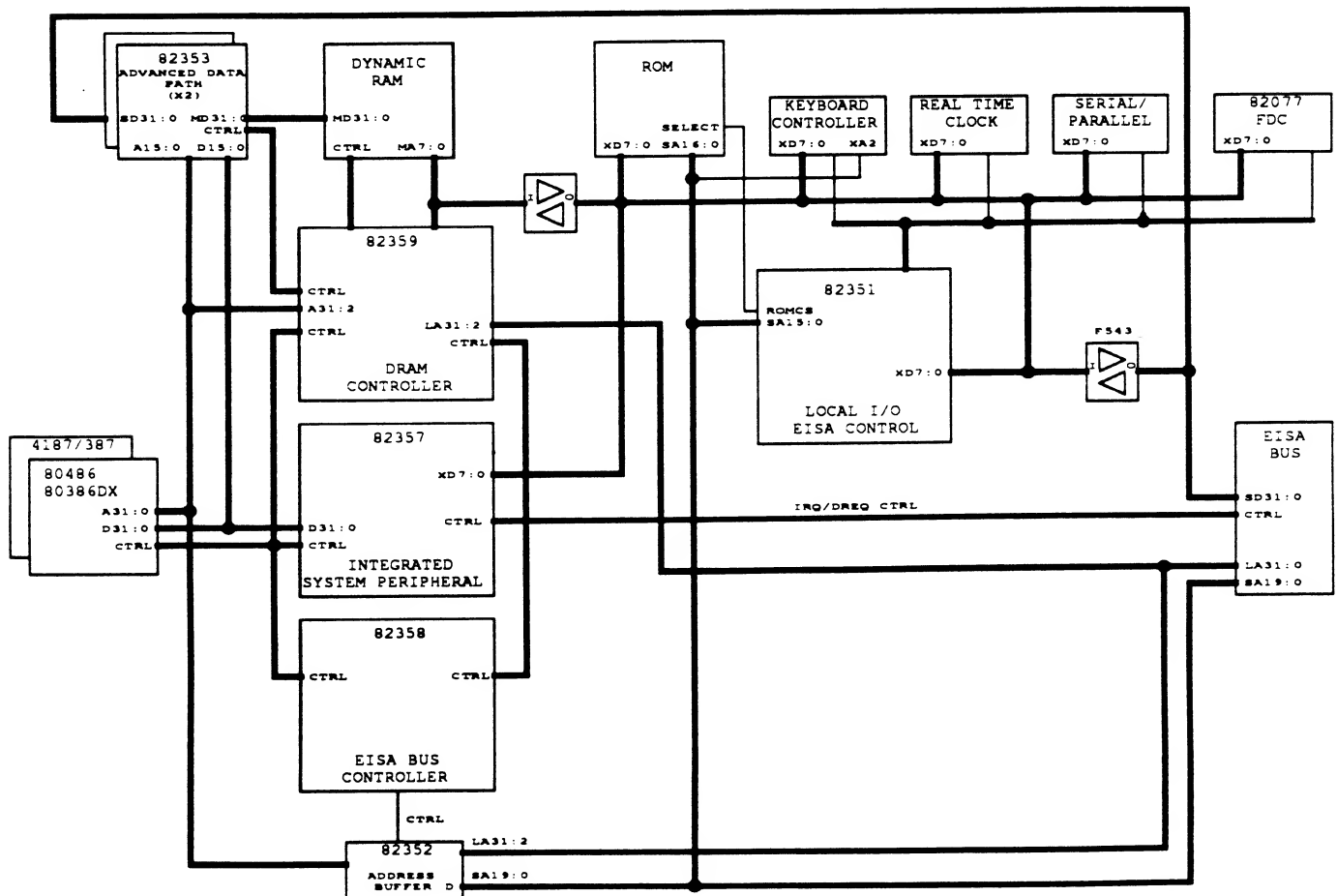
Keyboard/mouse interface

82077 floppy interface

Real-time clock

(4) user-programmable chip selects

IDE interface

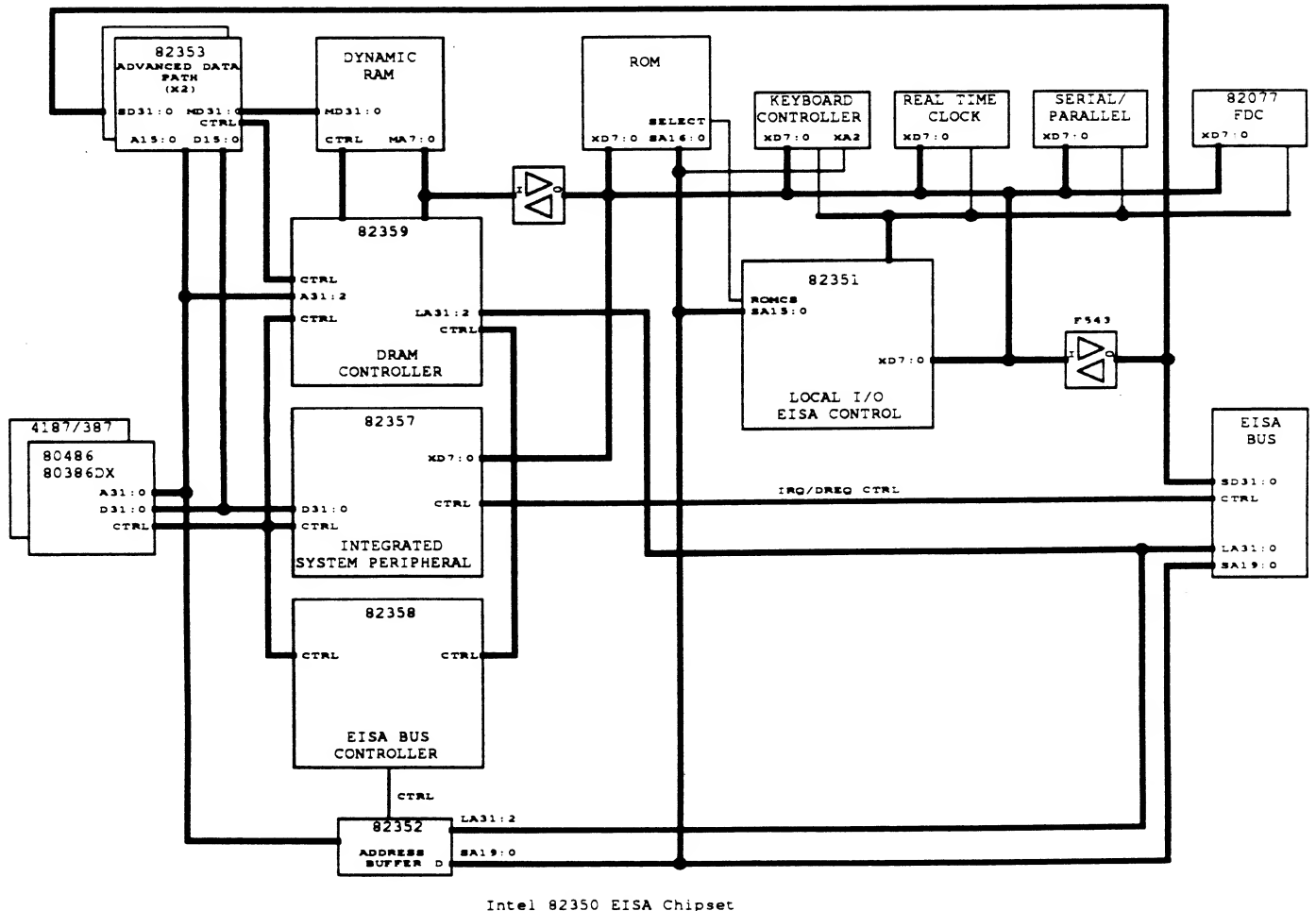


Intel 82350 EISA Chipset

## Personal Computer Design

**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386  
**System Bus:** EISA/ISA  
**Part:** 82352 EISA Bus Buffers  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
Data swap logic  
Address buffer  
Data parity buffer

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** No

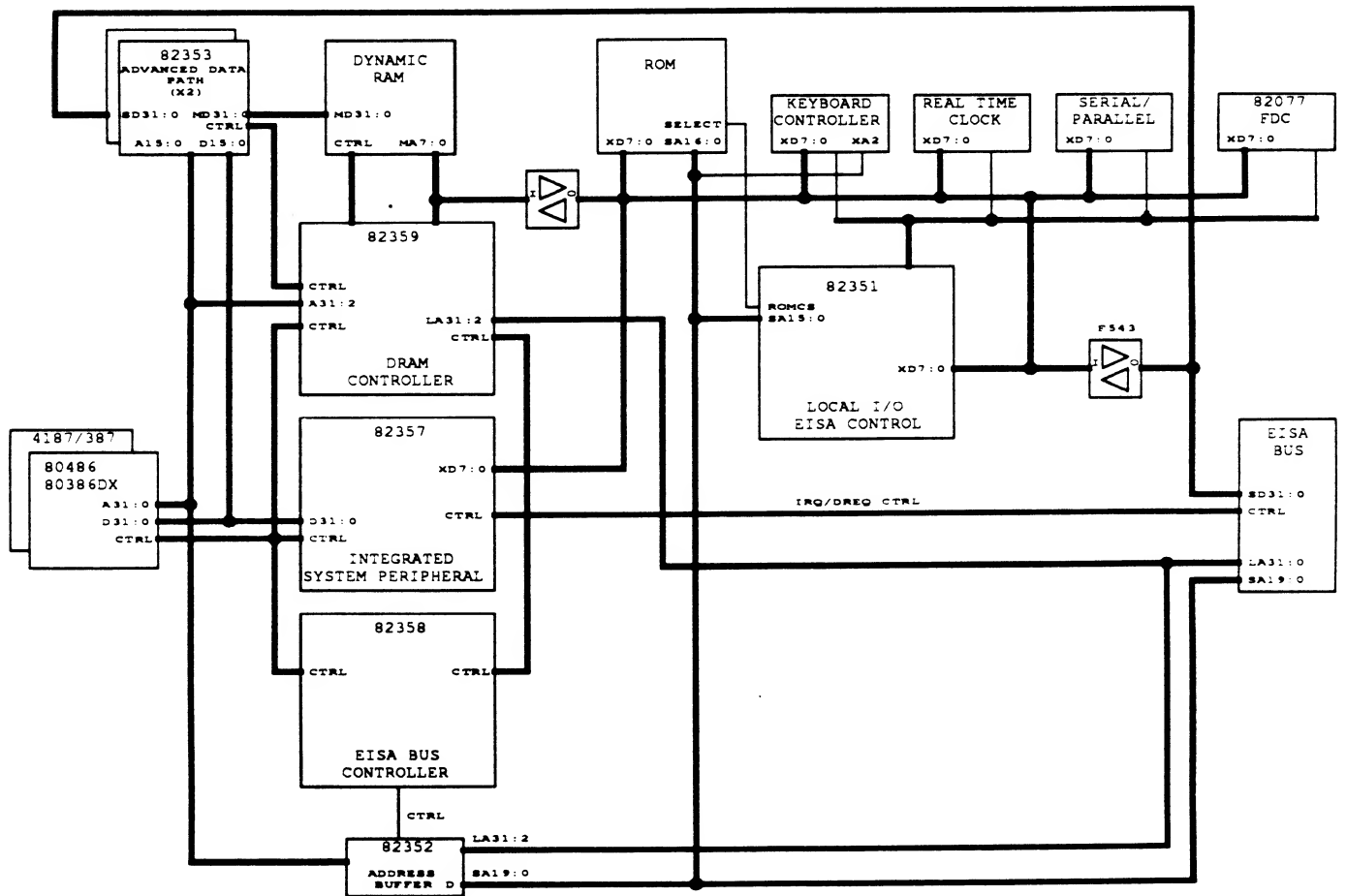


Intel 82350 EISA Chipset



**Manufacturer:** Intel  
**Processor Supported:** 80486  
**System Bus:** EISA/ISA  
**Part:** 82353 Advanced Data Path  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
 128-bit interface to main memory

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** No



Intel 82350 EISA Chipset

**Manufacturer:** Intel

**Processor Supported:** 80486, 80386

**System Bus:** EISA/ISA

**Part:** 82355 Bus Master Interface Controller

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

33MB/sec burst mode

EISA automatic configuration

2 identical transfer channels with 2 registers per channel

EISA interface

buffer interface

local interface

(2) 24-byte FIFOs

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**Cache Memory:** Yes

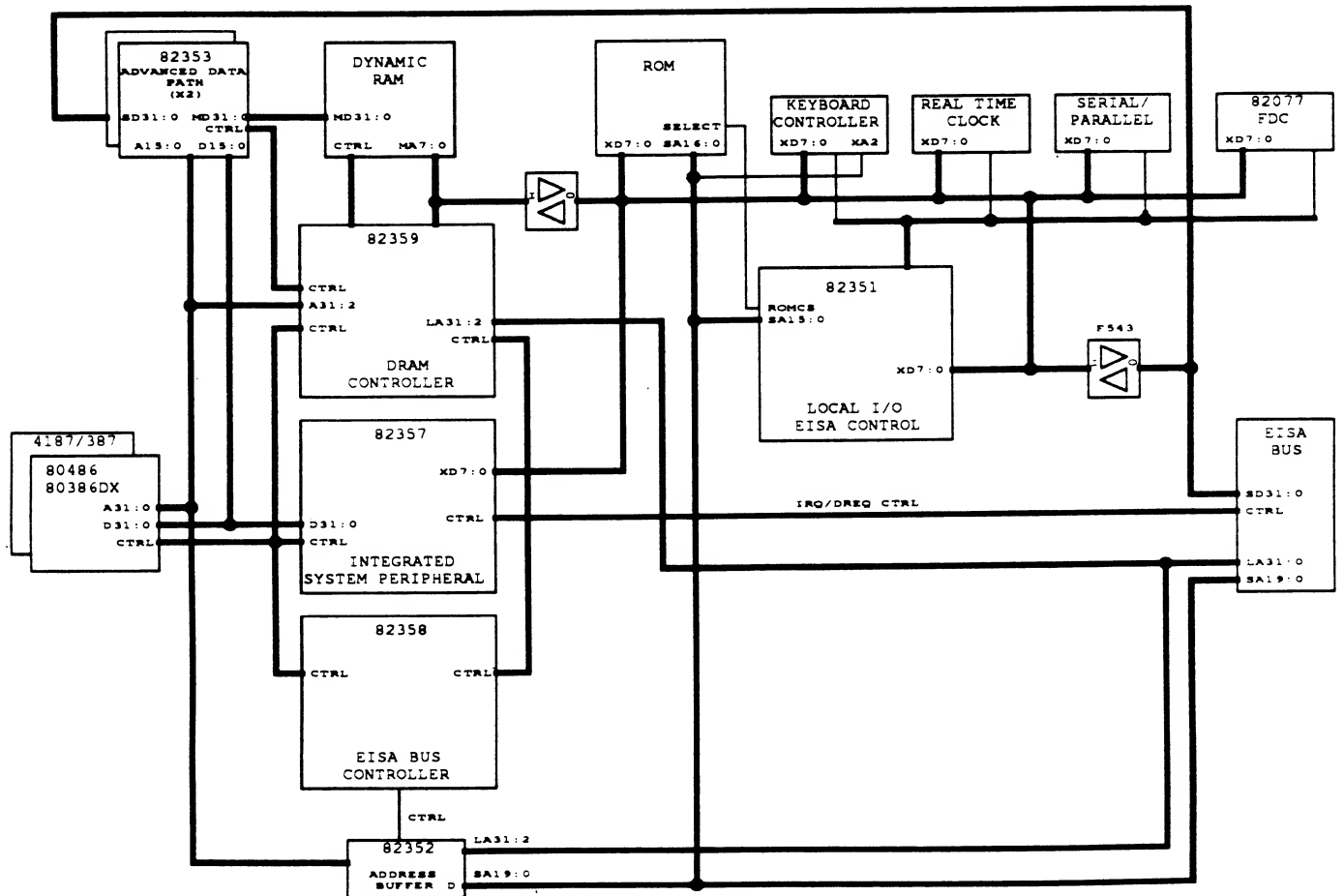
**Clock Speed:** NA

**Main Memory Support:** Yes, 4 GB

Schematic Not Available At Press Time

**Manufacturer:** Intel  
**Processor Supported:** 80386DX, 80486  
**System Bus:** EISA  
**Part:** 82357, Integrated System Peripheral (ISP)  
**Availability:** 1990  
**Second Source:** N/A  
**Functions Contained:**  
 (2) compatible 82C59A  
 (2) compatible 82C37A  
 (5) programmable timers (inc. 8254 compatible timer)  
 ISA/EISA DMA compatible cycles  
 Supports Type A/B/C cycle types  
 33 MBytes max transfer rate  
 Supports refresh  
 NMI control logic

**Cache Memory:** No  
**Clock Speed:** 25 & 33 MHz  
**Main Memory Support:** No



Intel 82350 EISA Chipset

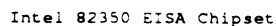
**Cache Memory:** No  
**Clock Speed:** 25 & 33 MHz  
**Main Memory Support:** No

### Functions Contained:

## Interfaces with 82357 and 82385

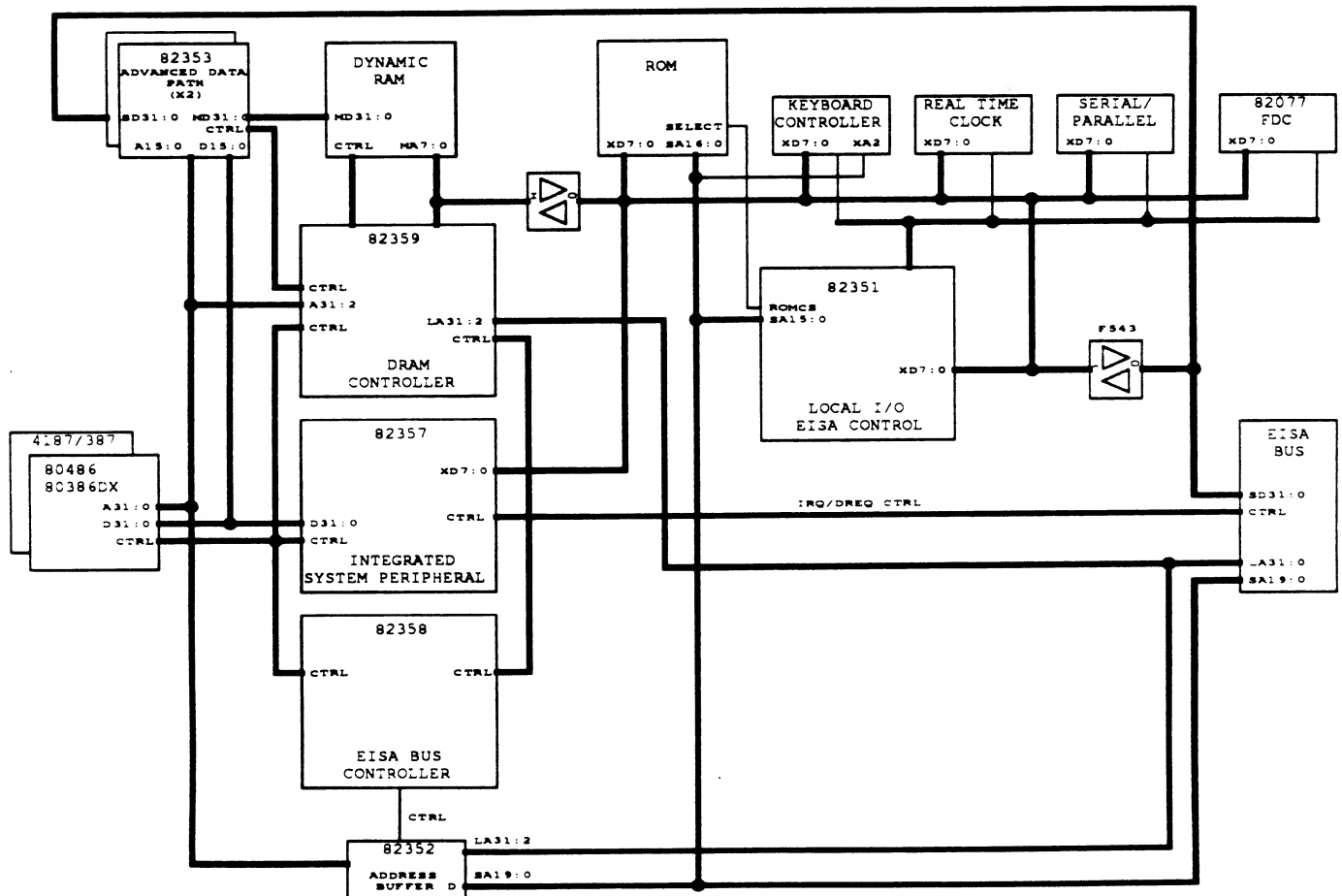
**Generates address and data buffers' control signals**

## Supports EISA/ISA Masters



**Manufacturer:** Intel  
**Processor Supported:** 80486, 80386  
**System Bus:** EISA/ISA  
**Part:** 82359 DRAM controller  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
 Dual-port access to main memory  
 Independent of CPU speed  
 80486 burst reads and posted writes at zero wait state

**Cache Memory:** No  
**Clock Speed:** NA  
**Main Memory Support:** Yes

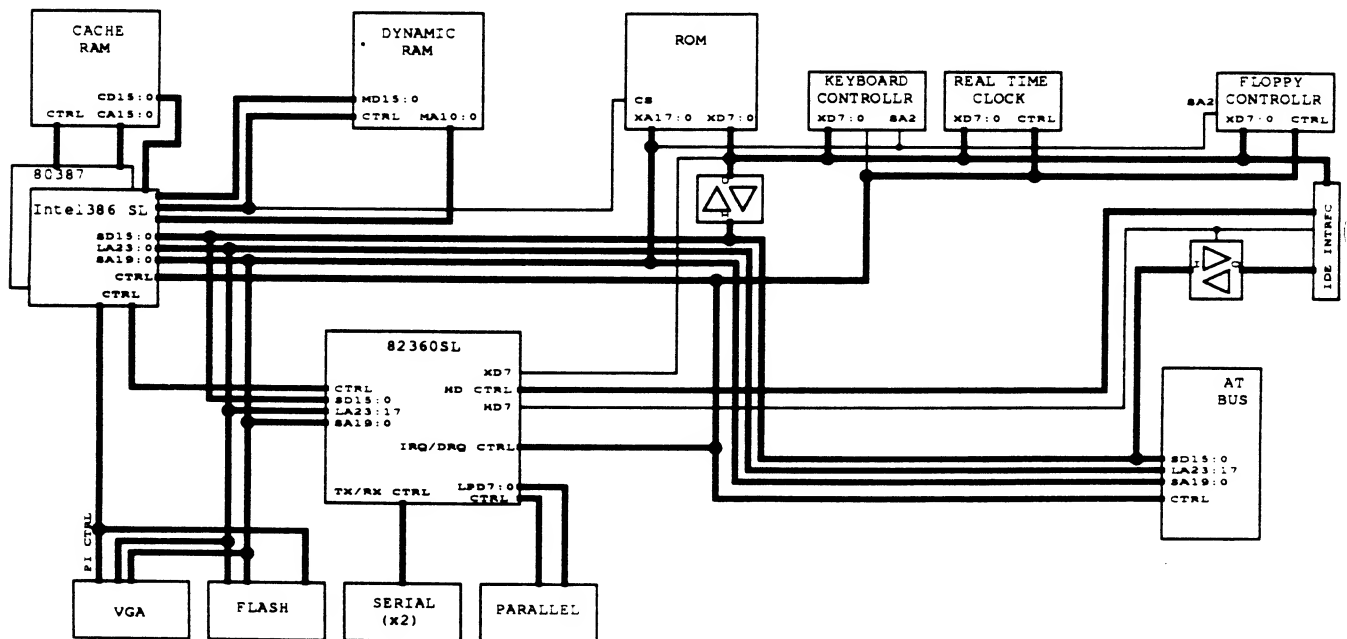


Intel 82350 EISA Chipset

## Personal Computer Design

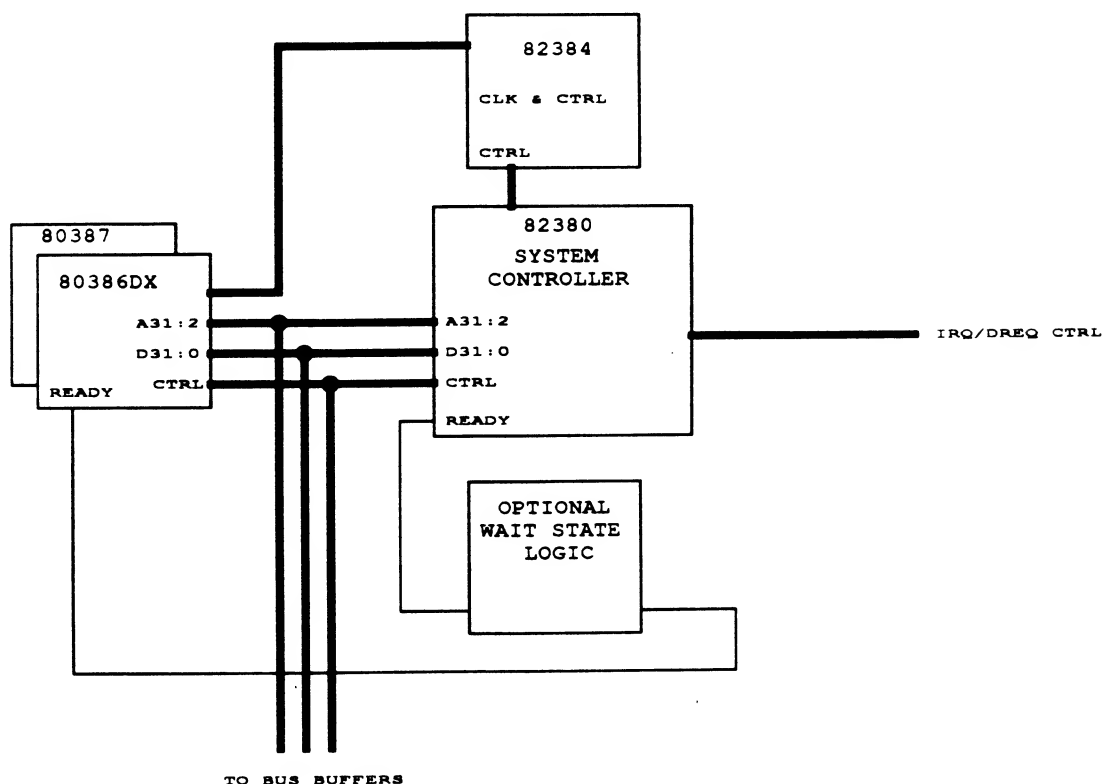
**Manufacturer:** Intel  
**Processor Supported:** Intel386 SL CPU  
**System Bus:** AT  
**Part:** 82360 SL  
**Availability:** 1991  
**Second Source:** N/A  
**Functions Contained:**  
Serial port  
Parallel port  
Timers  
Interrupt controller  
DMA controller  
Real time clock  
Supports keyboards/diskettes/IDE hard drives  
DRAM decoding/chip select logic  
Power management control logic

**Cache Memory:** No  
**Clock Speed:** 25 MHz (?)  
**Main Memory Support:** No



Intel 386 SL

**Manufacturer:** Intel  
**Processor Supported:** 80386DX  
**System Bus:** AT  
**Part:** 82380, High Performance 32-bit DMA Controller with Integrated System Support  
**Peripherals**  
**Availability:** 1987  
**Second Source:** N/A  
**Functions Contained:**  
 Supports 33 MBytes/sec DMA rate  
 (15) external & 5 internal interrupts supported  
 8259A superset  
 (4) 16-bit programmable timers (8254 compatible)  
 Shutdown detect/reset logic  
 Programmable wait state generator  
 Refresh control



Intel 82380 High Performance DMA Controller

**Manufacturer:** Intel

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** 82385, High Performance 32-bit Cache Controller

**Availability:** 1987

**Second Source:** MDS-C385i

**Functions Contained:**

99% Hit rates

Synchronous Dual Bus (snooping supported)

Supports upto 4 GB memory

Direct Map & 2-Way Set Associative Configurations

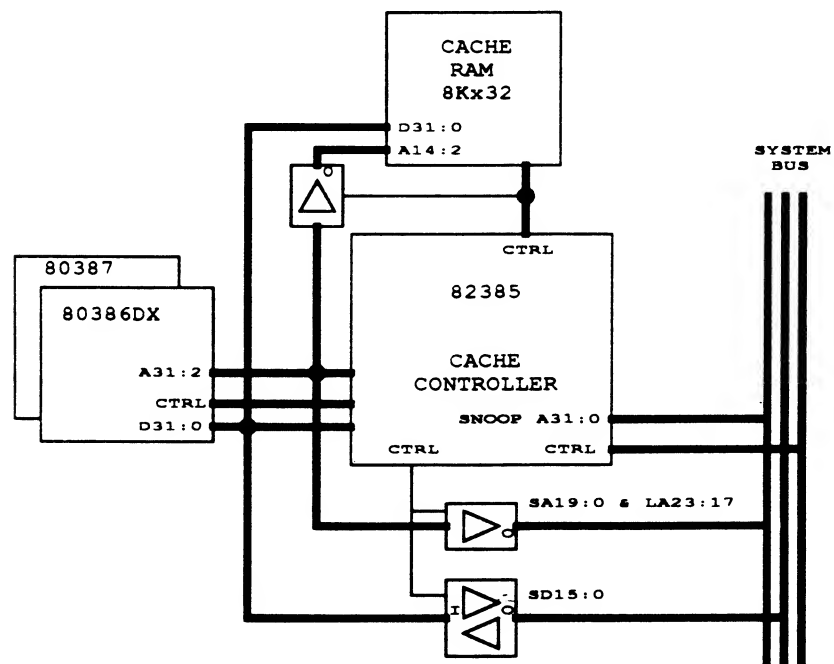
Supports non-cacheable area

---

**Cache Memory:** Yes

**Clock Speed:** 16 & 20 MHz

**Main Memory Support:** Yes

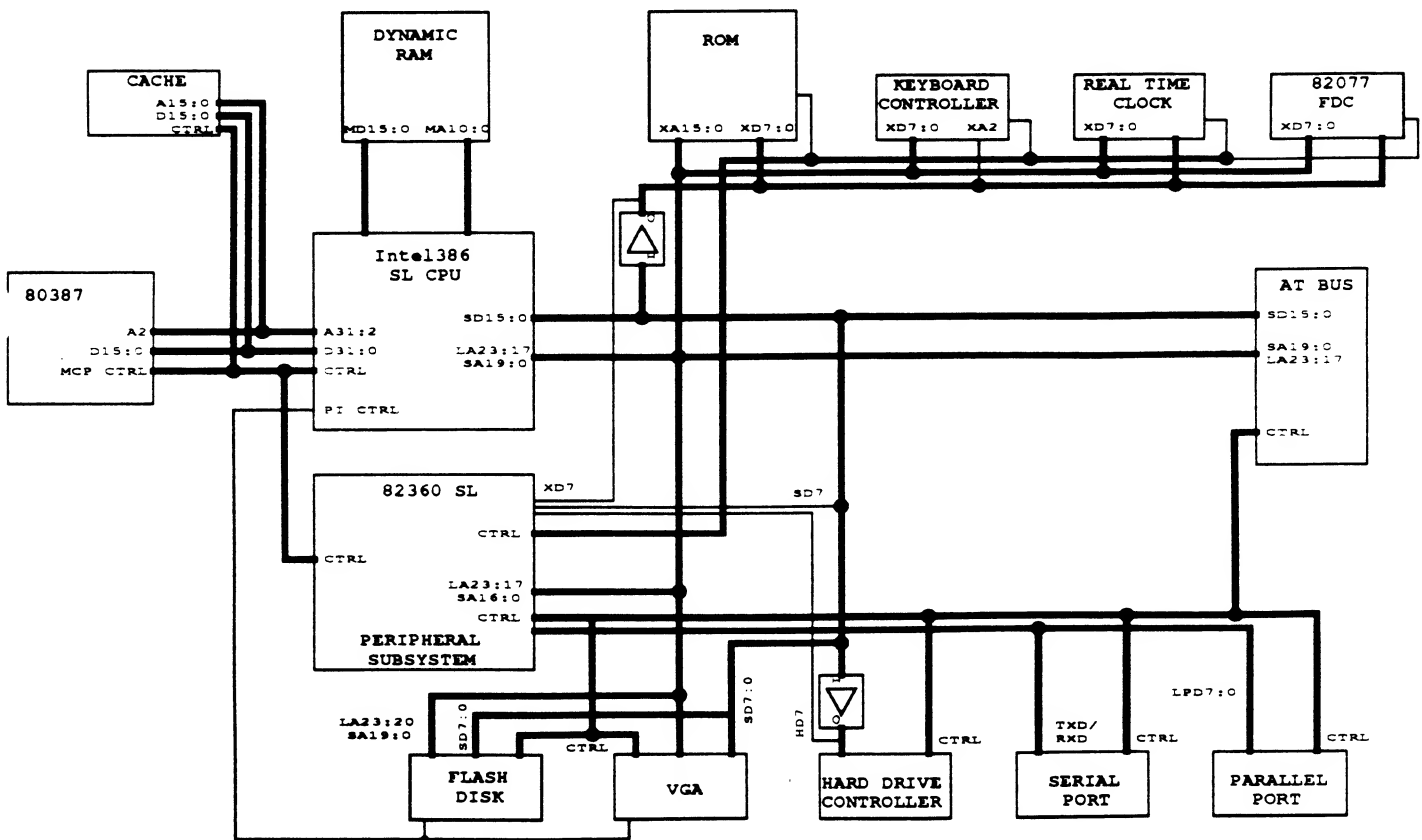


Intel 82385 32-bit Cache Controller  
Direct Mapped Configuration



**Manufacturer:** Intel  
**Processor Supported:** N/A (80386 compatible itself)  
**System Bus:** AT  
**Part:** Intel386 SL CPU  
**Availability:** 1991  
**Second Source:** N/A  
**Functions Contained:**  
 Intel 80386 compatible  
 Reduced run-time power requirements  
 Supports LIM 4.0 EMS  
 Supports ROM shadowing  
 Supports 20 MB main memory and 32 MB external  
 Supports ISA bus and high performance Peripheral Interface bus

**Cache Memory:** No  
**Clock Speed:** 25 MHz (?)  
**Main Memory Support:** Yes



Intel386 SL Microprocessor SuperSet

## **Personal Computer Design**

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**Manufacturer:** Intel

**Processor Supported:** 80386

**System Bus:** AT

**Part:** 82365SL PCMCIA Card Interface Controller

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

jumperless system configuration of ExCA card resources

Interfaces between ISA bus and PCMCIA socket

---

**Cache Memory:** No

**Clock Speed:** NA

**Main Memory Support:** ?

Schematic Not Available At Press Time

**Manufacturer:** Intel  
**Processor Supported:** 80386  
**System Bus:** EISA/ISA  
**Part:** 82395DX/82396SX Smart Cache  
**Availability:** NA  
**Second Source:** NA  
**Functions Contained:**  
Dual bus concurrency  
16 KB of SRAM  
4-way set associative  
4-deep read and write buffers  
Concurrent line buffer caching

**Cache Memory:** Yes  
**Clock Speed:** NA  
**Main Memory Support:** NA

Schematic Not Available At Press Time

**Manufacturer:** Intel

**Processor Supported:** 80486

**System Bus:** AT

**Part:** 82485 Cache Controller

**Availability:** NA

**Second Source:** NA

**Functions Contained:**

Integrated tag RAM

Zero-wait-state access with one clock bursting

Allows BIOS caching

---

**Cache Memory:** Yes

**Clock Speed:** 25, 33 Mhz

**Main Memory Support:** Yes, 4 GB

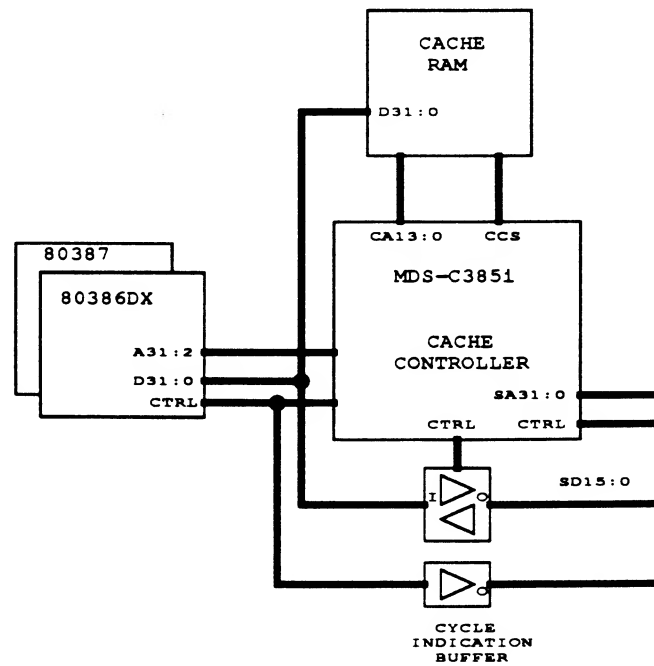
Schematic Not Available At Press Time

**Manufacturer:** MetaDesign Semiconductor  
**Processor Supported:** 80386DX  
**System Bus:** AT  
**Part:** MDS-C385i, 32KB 32 bit Cache controller  
**Availability:** May 1990  
**Second Source:** ?

**Cache:** Yes  
**Clock Speed:** 20, 25, & 33 MHz  
**Main Memory Support:** No

**Functions Contained:**

Plug compatible with Intel 82385  
 Direct and 2-way set associative memory map support  
 Supports write through scheme



MATRA MDS-C3851

**Manufacturer:** MetaDesign Semiconductor

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** MDS-C390, Advanced 32-bit Cache Controller

**Availability:** May 1990

**Second Source:** none

**Functions Contained:**

Supports 32KB, 64KB, 128KB, & 256KB Cache systems

Write through updating scheme

Direct and 2-way/4-way set associative memory map support

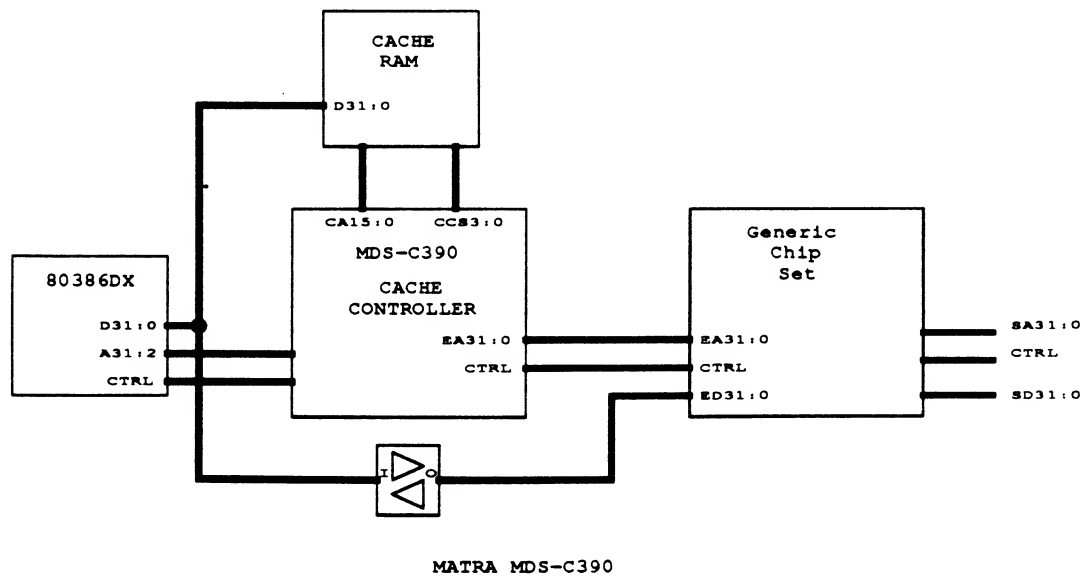
Direct interface to standard high speed SRA bus

---

**Cache:** Yes

**Clock Speed:** 20, 25, & 33 MHz

**Main Memory Support:** No



**Manufacturer:** MetaDesign Semiconductor

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** MDS-C395e, Copy-Back/Write-Thru 32-bit Cache Controller

**Availability:** May 1990

**Second Source:** none

**Functions Contained:**

Supports 32KB, 64KB, 128KB, & 256KB Cache systems

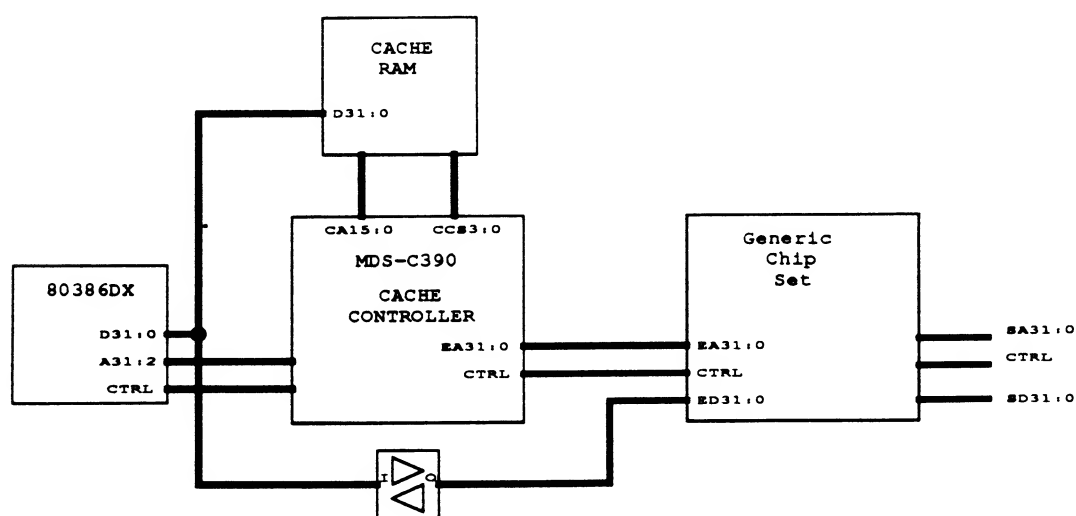
Write through scheme with posted writes

Direct and 2-way/4-way set associative memory map support

**Cache:** Yes

**Clock Speed:** 20, 25, & 33 MHz

**Main Memory Support:** No



MATRA MDS-C390

**Manufacturer:** MetaDesign Semiconductor

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** MDS-C415 Cache interface Adapter

**Availability:** 1992

**Second Source:** MHS

**Functions Contained:**

Clock & Reset generator for 80486

Clock generator for MDS-395e

Address control lines (fills from secondary to primary cache)

---

**Cache:** Yes

**Clock Speed:** 25 & 33 MHz

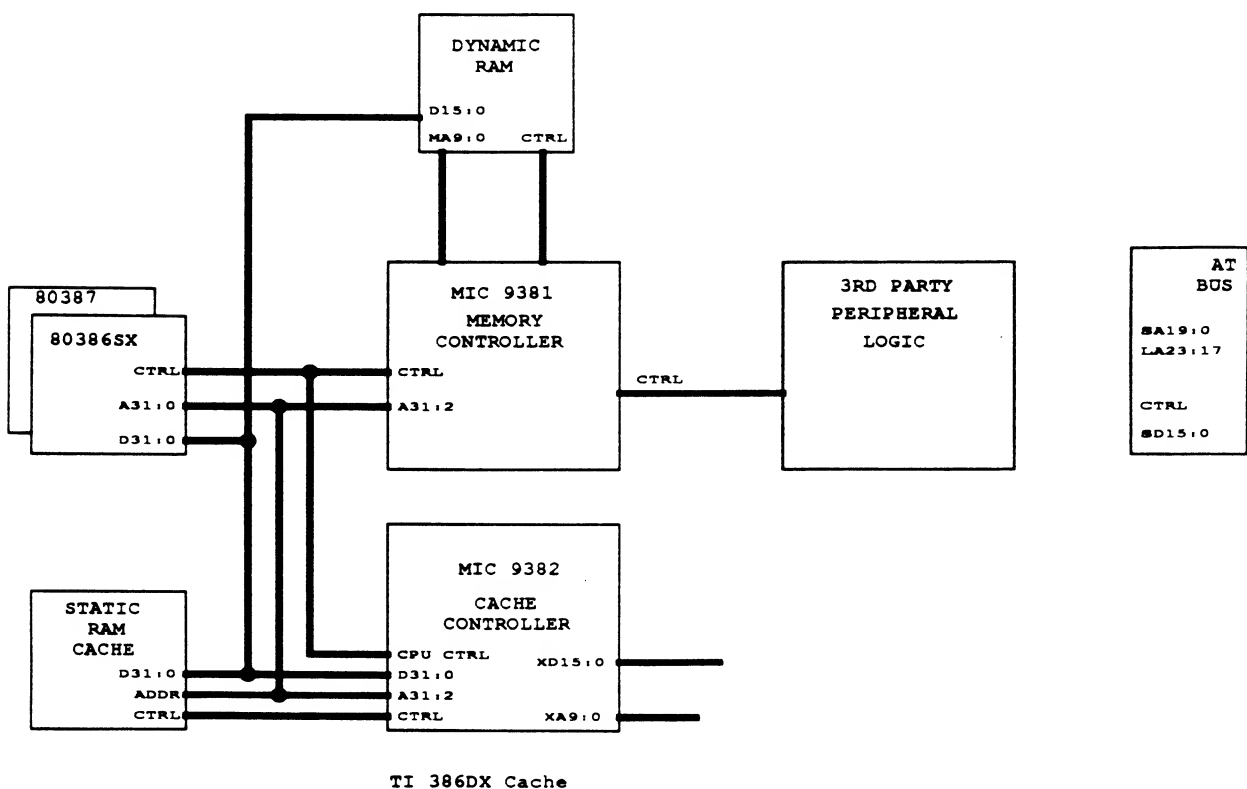
**Main Memory Support:** No

Schematic Not Available At Press Time



**Manufacturer:** Micro Integration Corporation  
**Processor Supported:** 80386  
**System Bus:** AT  
**Part:** MIC9381, CPU & Cache Controller  
**Availability:** 1989  
**Second Source:** ?  
**Functions Contained:**  
 CPU/AT Bus Controller  
 Clock Generator  
 32KB, 64KB, 128KB Mapped Cache control

**Cache:** Yes  
**Clock Speed:** 25 or 33 MHz  
**Main Memory Support:** No



**Manufacturer:** Micro Integration Corporation

**Processor Supported:** 80386

**System Bus:** AT

**Part:** MIC9382, Memory Controller

**Availability:** 1989

**Second Source:** ?

**Functions Contained:**

Multiple Interleaved Paging (MIP) memory controller

Programmable DRAM memory wait state logic

Shadow RAM

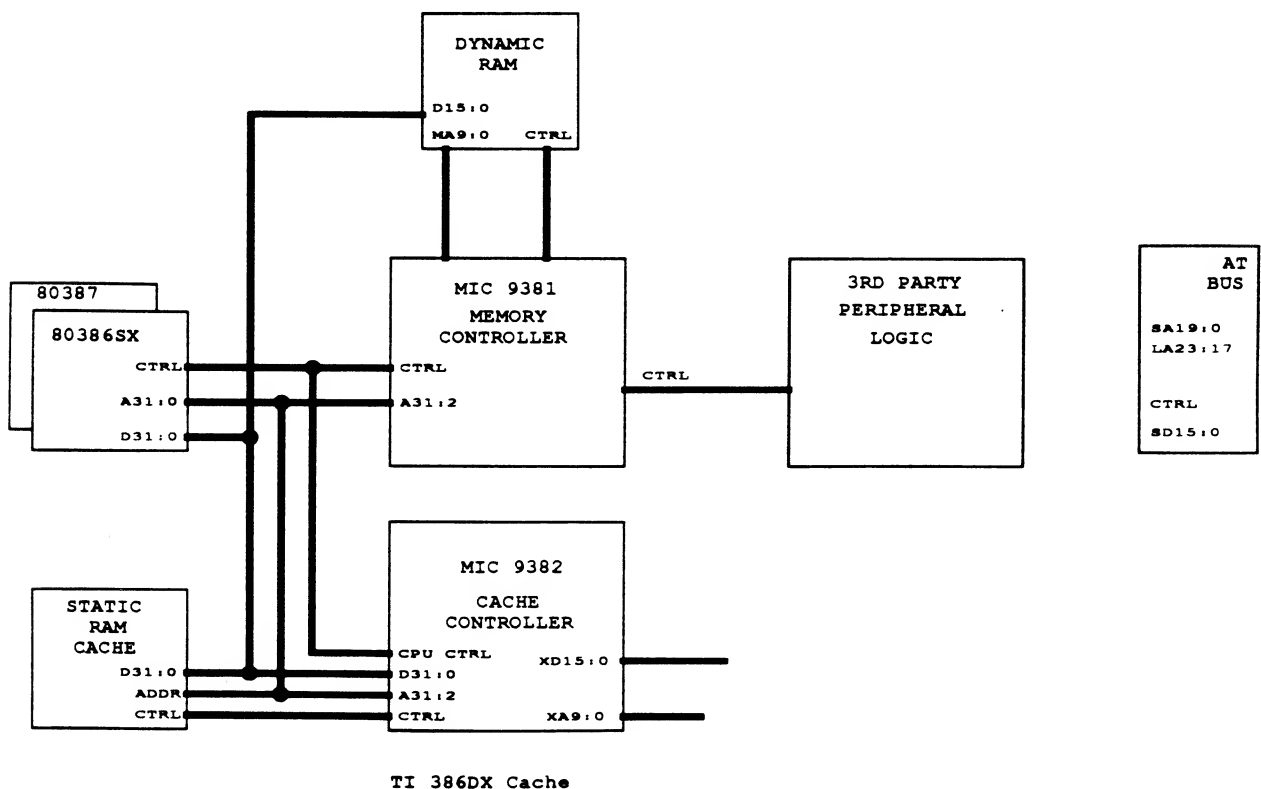
Gate A20 support

---

**Cache:** No

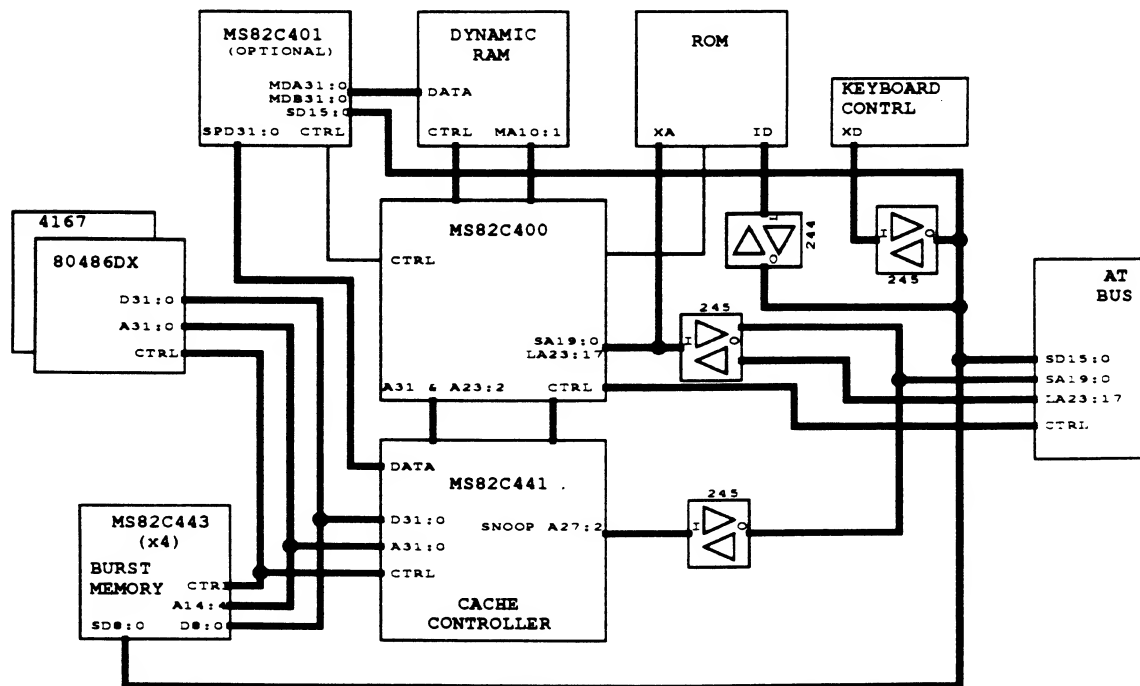
**Clock Speed:** 25/33 MHz

**Main Memory Support:** Yes



**Manufacturer:** Mosel  
**Processor Supported:** 80486SX, 80486DX  
**System Bus:** AT, EISA  
**Part:** MS400, Single Chip AT  
**Availability:** Q4 1991  
**Second Source:** none  
**Functions Contained:**  
 DRAM Controller  
 Interrupt Controllers  
 Timer  
 DMA Controller  
 Memory Mapper  
 All other logic "basic to" an AT based computer

**Cache:** No  
**Clock Speed:** 20 to 33 MHz  
 50 MHz with SimulCache  
**Main Memory Support:** Yes



Mosel MS400 486SX/DX SINGLE CHIP AT

## Personal Computer Design

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**Manufacturer:** Mosel

**Processor Supported:** 80386DX, 80486DX, 80486SX

**System Bus:** AT

**Part:** MS401, 32/64 bit Data Path Chip

**Availability:** Q4 1991

**Second Source:** ?

**Functions Contained:**

Replaces 17 standard buffer devices used in 486 motherboards

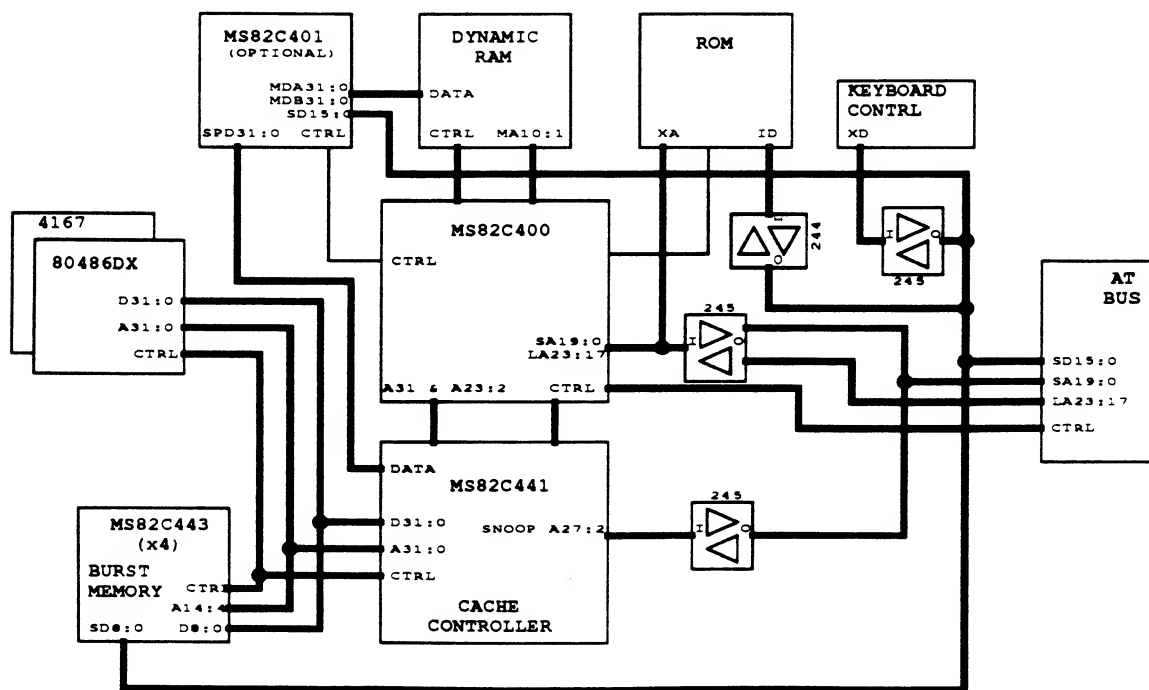
Supports 4 bit Parity

---

**Cache:** No

**Clock Speed:** ? MHz

**Main Memory Support:** No



Mosel MS400 486SX/DX SINGLE CHIP AT

**Manufacturer:** Mosel

**Cache:** Yes

**Processor Supported:** 80386, 80486, Weitek 4167 **Clock Speed:** 25 & 33 MHz (0 Wait)

**System Bus:** AT, EISA

**Main Memory Support:** No

**Part:** MS441, SimulCache Controller (Concurrent Write Back Cache)

**Availability:** Q4 1991

**Second Source:** ?

**Functions Contained:**

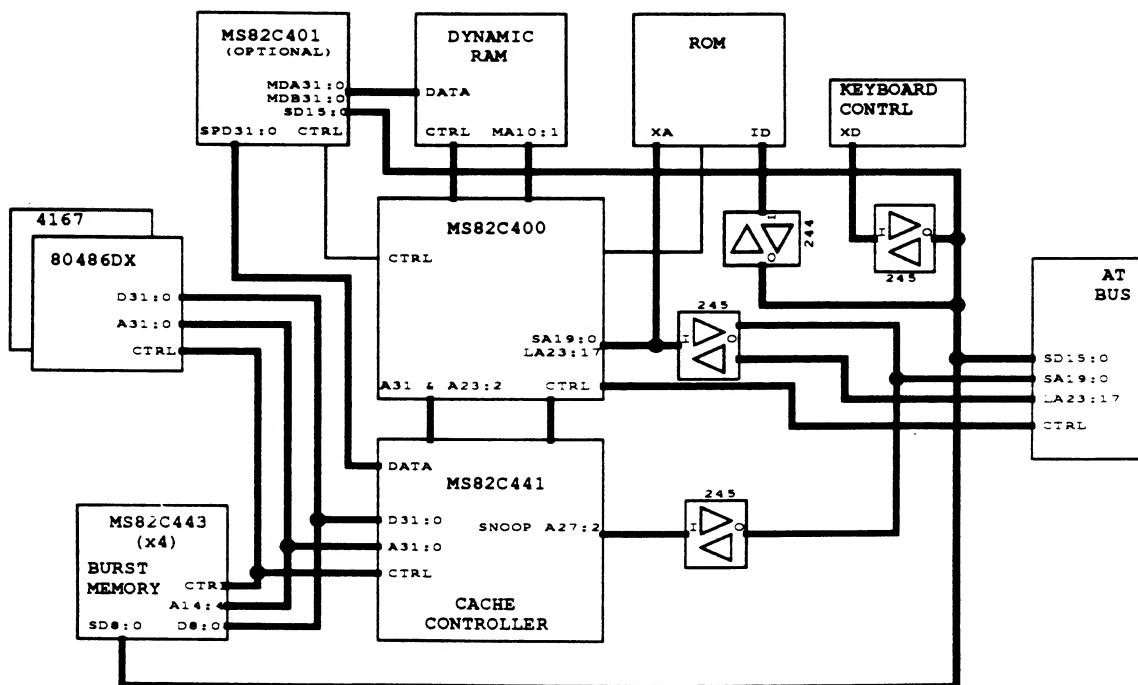
Integrated Tag Array (2000 entries)

System/Local Bus Controller (Dual Concurrent)

Allows bursting of reads from system memory

Data Path Control

Concurrent Bus Control Unit



Mosel MS400 486SX/DX SINGLE CHIP AT

**Cache:** Yes

**Processor Supported:** 80386, 80486

**Clock Speed:** 25 & 33 MHz (0 Wait)

**System Bus:** AT

**Main Memory Support:** No

**Part:** MS443, Burst Memory (High Performance, Dual Port, Intelligent)

**Availability:** Q4 1991

**Second Source:** ?

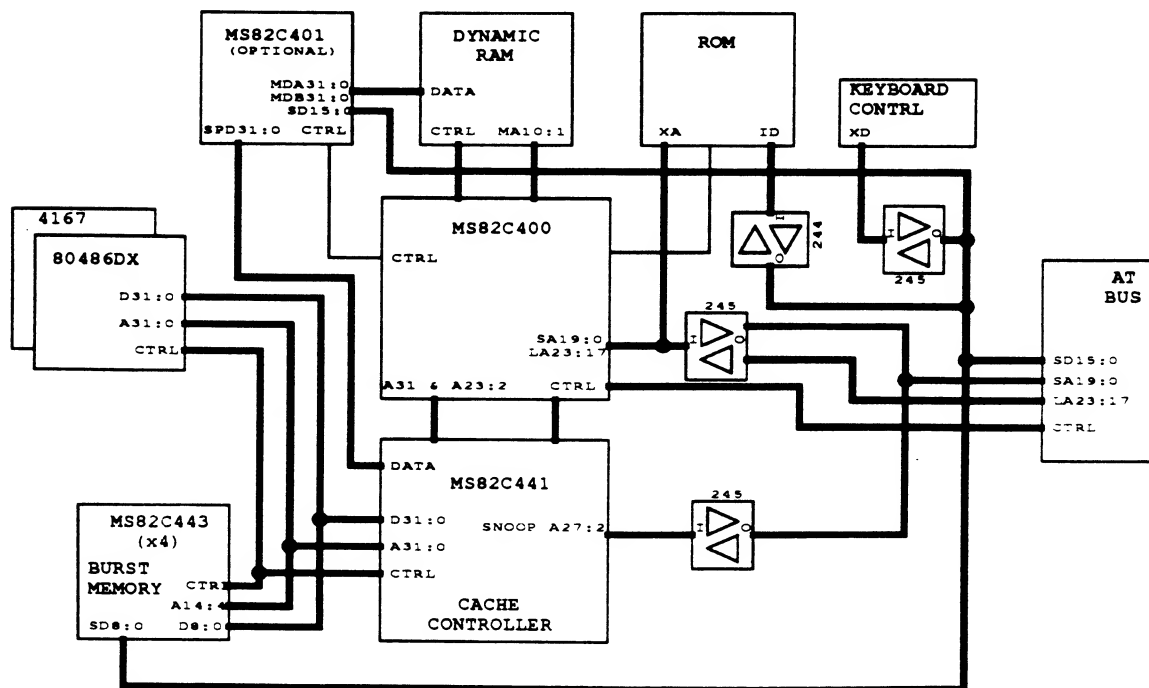
**Functions Contained:**

144K bit memory (64KB = two sets of four banks, with 2Kx9 per bank)

Concurrent Dual Bus Access (256 MBytes/sec)

Intelligent Hit/Miss Caching Logic

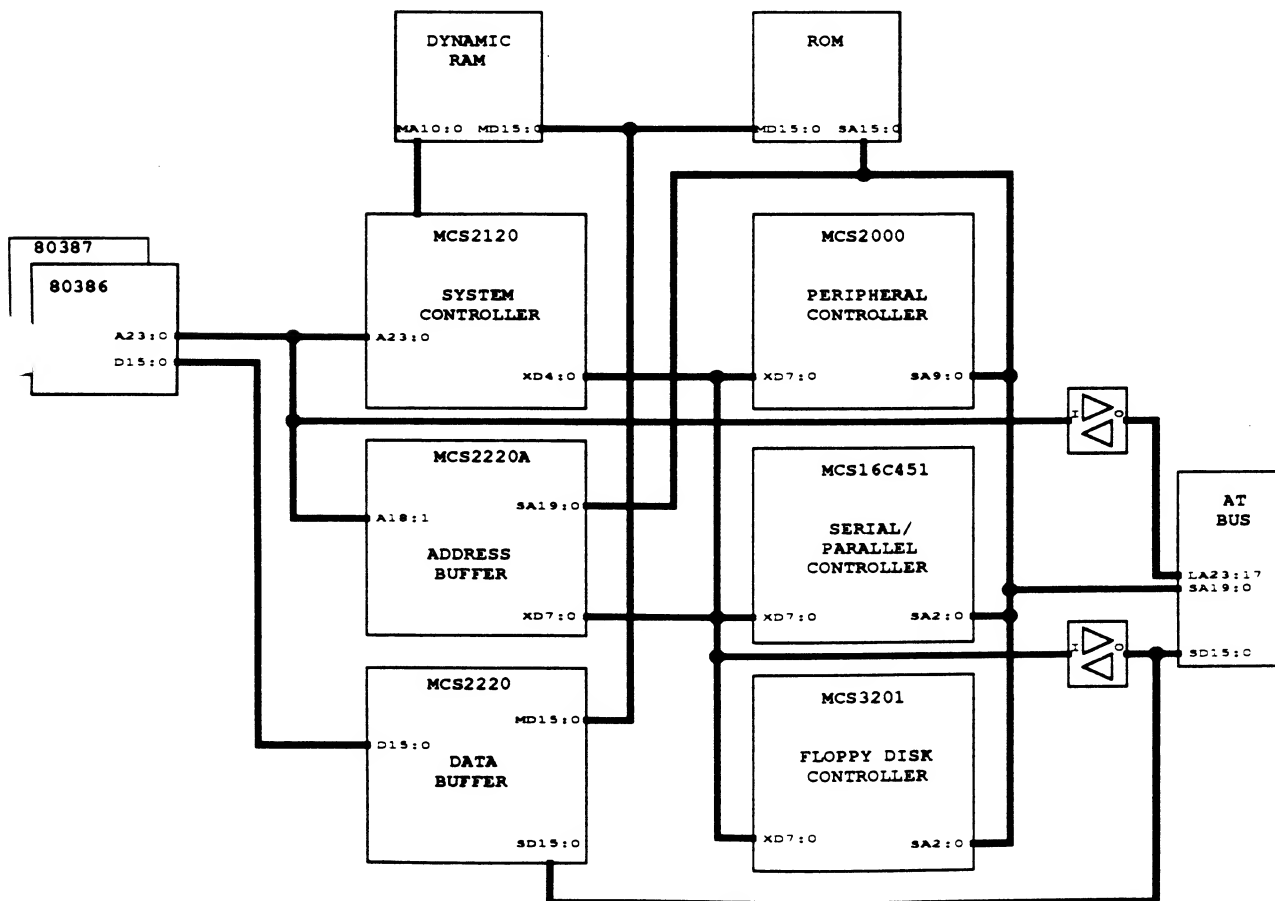
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Model MS400 486SX/DX SINGLE CHIP AT

**Manufacturer:** Motorola  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT, EISA  
**Part:** MCS2000, Peripheral Controller  
**Availability:** 1989  
**Second Source:** ?  
**Functions Contained:**  
 (two) 8237 DMA Controllers  
 (two) 8259A Interrupt Controllers  
 (one) 8254 timer/counter  
 (one) 74LS612 memory mapper.

**Cache:** No  
**Clock Speed:** 12/16 MHz  
**Main Memory Support:** No



Motorola MCS82020 Turbo PC/AT Chipset

## Personal Computer Design

**Manufacturer:** Motorola

**Processor Supported:** 80286, 80386SX

**System Bus:** AT, EISA

**Part:** MCS2120, PC/AT Integrated System Controller

**Availability:** 1989

**Second Source:** ?

**Functions Contained:**

82284 Clock Generator

80287 Interface Control

4 way, Page Interleaved Memory Controller

Configuration Registers

ROM Chip Select Logic (for 27128 & 27256)

**Cache:** No

**Clock Speed:** 16 MHz (0 wait)  
20 MHz (1 Wait)

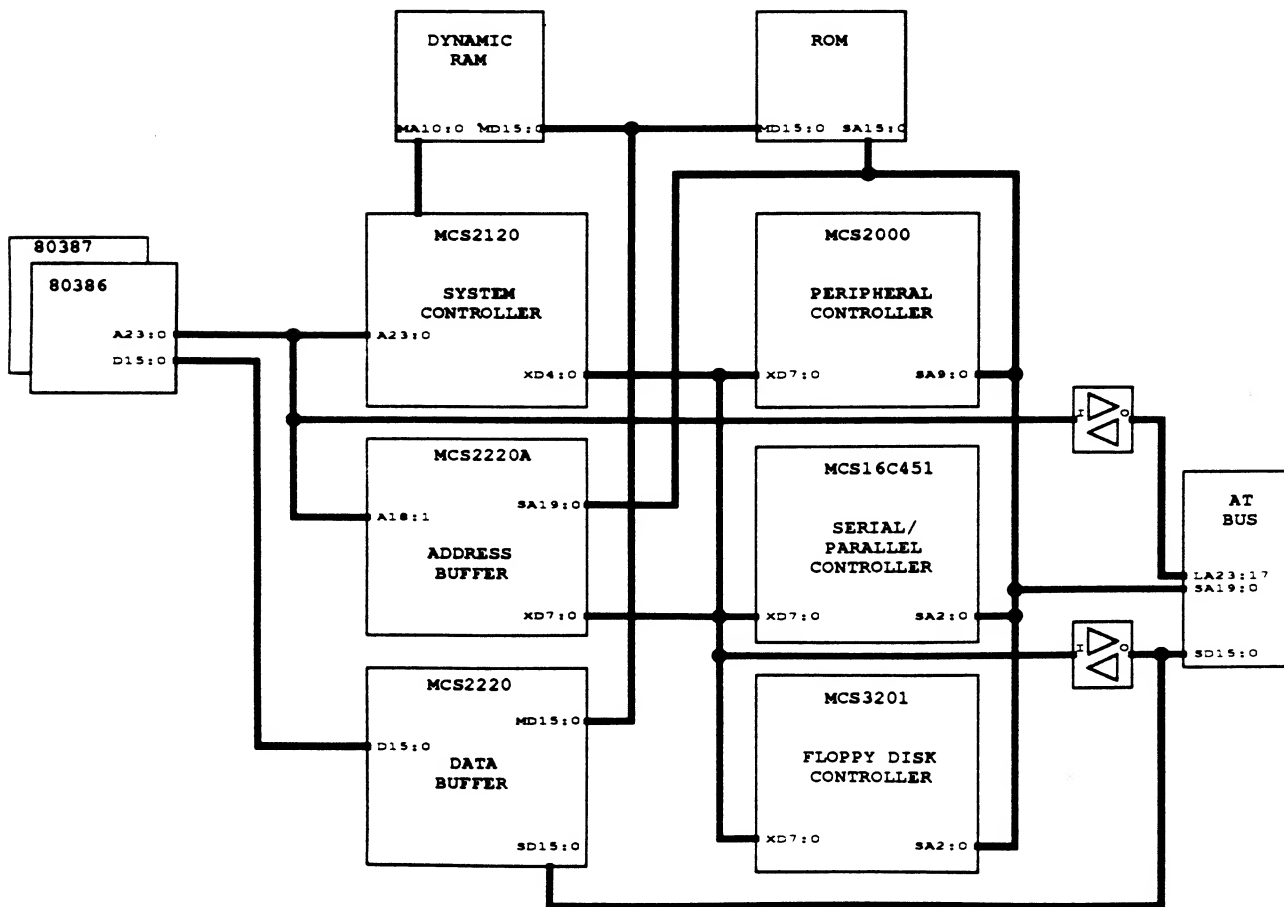
**Main Memory Support:** No

82288 Bus Controller/Converter

Wait State Generator

Turbo Speed Control Logic

Shut Down circuitry



Motorola MCS82020 Turbo PC/AT Chipset



**Manufacturer:** Motorola

**Processor Supported:** 80286, 80386SX

**System Bus:** AT, EISA

**Part:** MCS2220/2220A Data Latch & Address Latch/Buffer

**Availability:** 1989

**Second Source:** ?

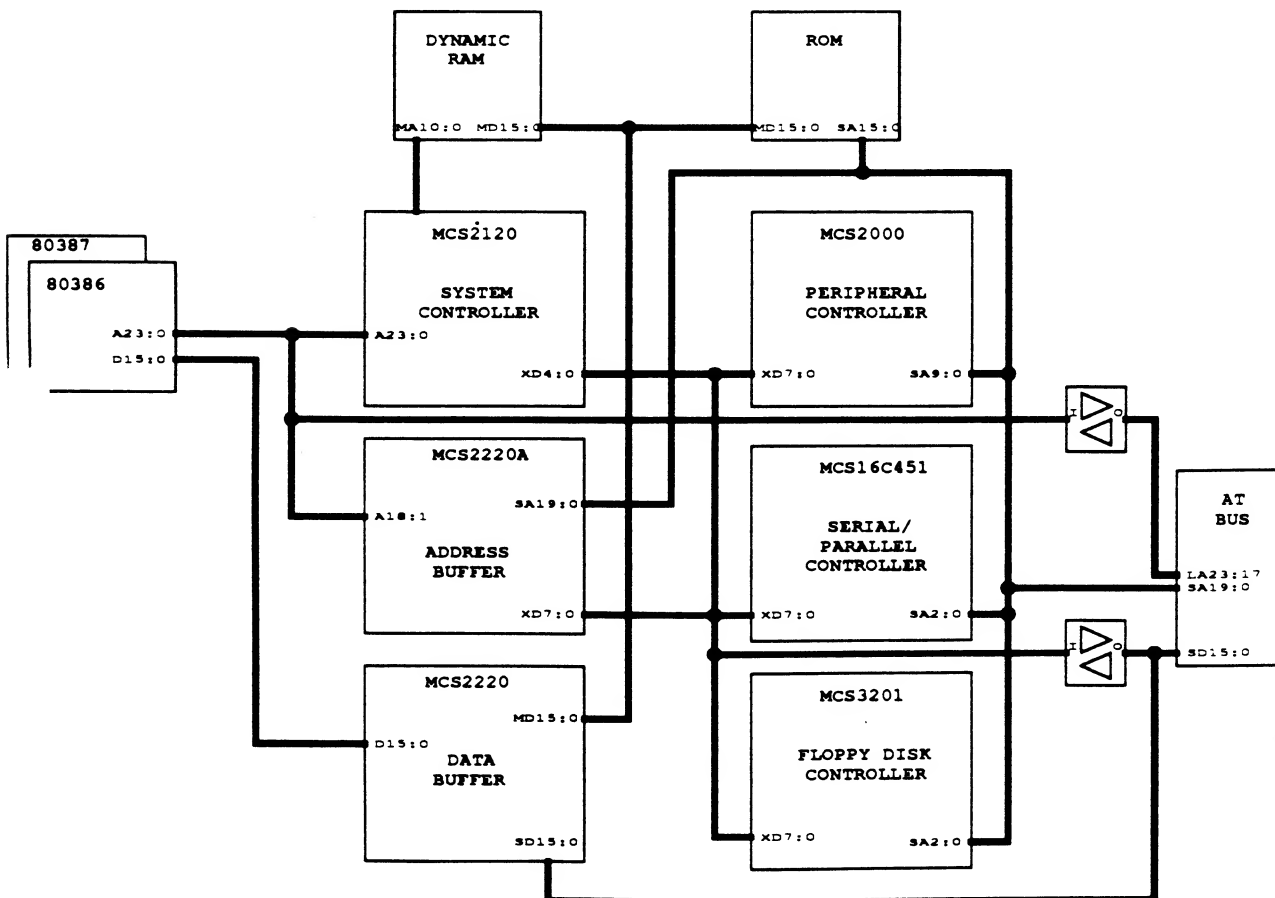
**Functions Contained:**

Provides 74LS244 and 74LS573 compatibility

**Cache:** No

**Clock Speed:** 12/16 MHz

**Main Memory Support:** No



Motorola MCS82020 Turbo PC/AT Chipset

**Manufacturer:** Motorola

**Processor Supported:** 80386

**Cache:** No

**Clock Speed:** 20 MHz (0 wait)  
20 Mhz (1 wait)

**System Bus:** AT, EISA

**Main Memory Support:** Yes

**Part:** MCS2300, CMOS Page/ Page Interleaved Memory Controller

**Availability:** 1989

**Second Source:** ?

**Functions Contained:**

Page interleaved or direct DRAM accessed

Shadow RAM

Staggered refresh

---

Schematic Not Available At Press Time

**Manufacturer:** National Semiconductor

**Processor Supported:** 80286, 80386

**System Bus:** PC, XT, AT, PS/2 (micro channel)

**Part:** PC16553, Dual UARTS with FIFO & high performance parallel interface

**Availability:** 1990

**Second Source:** ?

**Functions Contained:**

(2) UARTS (compatible with INS8250A, NS16450, & NS16550AF)

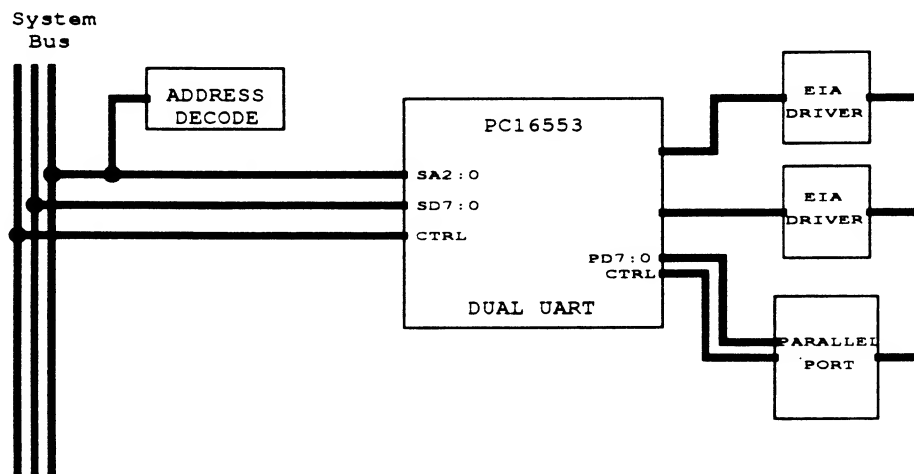
Divide by 13 clock

---

**Cache:** No

**Clock Speed:** ? MHz

**Main Memory Support:** No



National Semiconductors PC16553

## **Personal Computer Design**

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**Manufacturer:** National Semiconductor

**Processor Supported:** 80286, 80386

**System Bus:** AT, EISA, PS/2 (micro channel)

**Part:** PC8477, Advanced Floppy Disk Controller

**Availability:** 1990

**Second Source:** ?

**Functions Contained:**

Software compatible with NEC mPD765 & National DP8473

Pin & software compatible with N82077

Perpendicular mode recording

DMA control circuitry

separator

1MB/s transfer rate support

**Cache:** No

**Clock Speed:** 24 MHz (Xtal)

**Main Memory Support:** No

16 byte FIFO

write precompensation

High Performance internal data

Power Down mode

---

Schematic Not Available At Press Time

**Manufacturer:** National Semiconductor  
**Processor Supported:** 80286  
**System Bus:** AT, EISA, PS/2 (micro channel)  
**Part:** PC87120, SuperAT

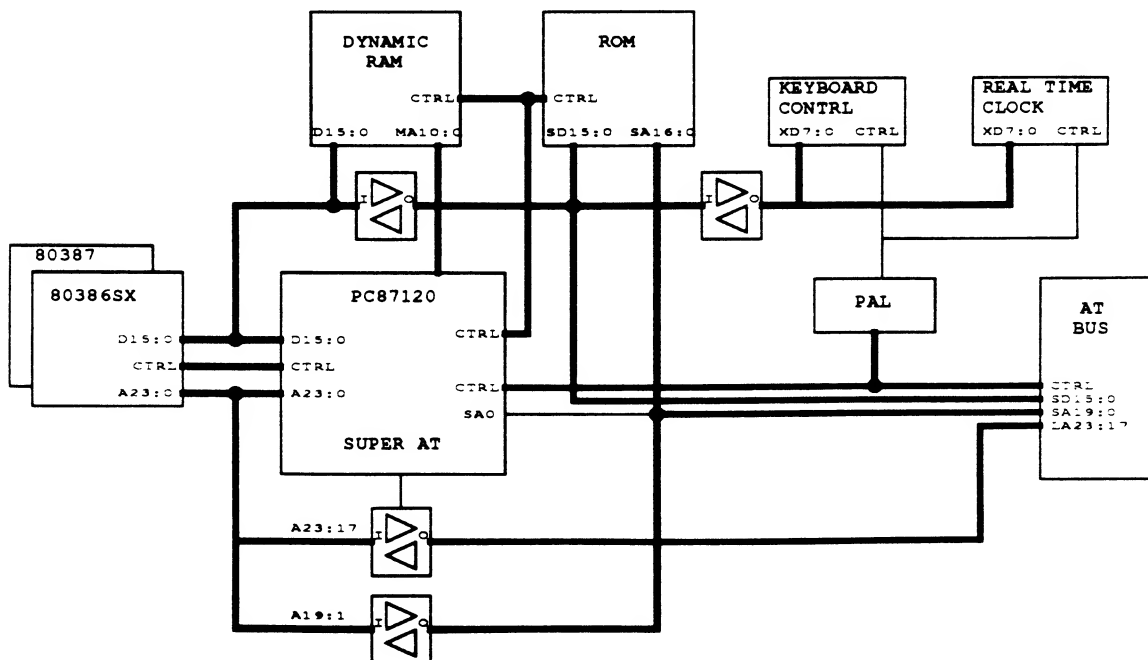
**Cache:** No  
**Clock Speed:** 10 - 16 MHz  
**Main Memory Support:** Yes

**Availability:** 1991

**Second Source:** None

**Functions Contained:**

Memory controller supports conventional mode, page mode or 2-way page interleaving	Software configurable Wait States
Supports 512KB to 8MB DRAM	Fast GateA20 support
Supports shadow RAM of BIOS	Programmable synch/asynch expansion bus
Power down, sleep, & slow refresh	Staggered refresh
8-bit/16-bit BIOS ROM select switch	(2) compatible 8237 DMA controllers
Hardware/software selectable CPU speed	(1) 8254 compatible Timer/Counter
(2) compatible 8259 Interrupt controllers	
(1) 75LS612 compatible memory mapper	



National Semiconductor PC87120 SuperAT Chipset

## Personal Computer Design

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**Manufacturer:** National Semiconductor  
**Processor Supported:** 80386SX  
**System Bus:** AT, EISA, PS/2 (micro channel)  
**Part:** PC87130, SuperAT/SX

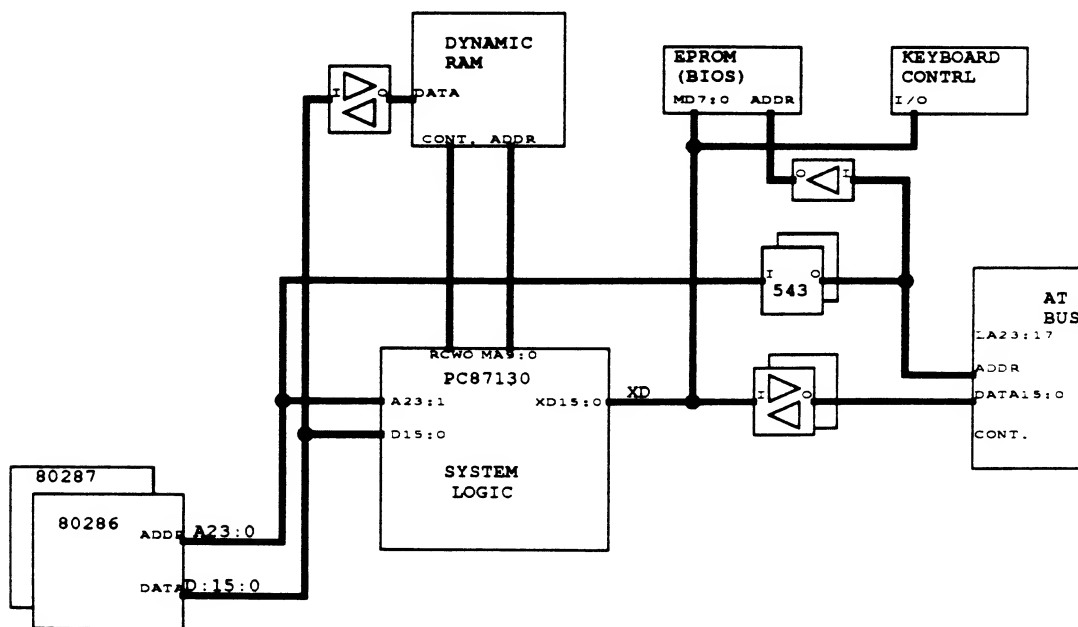
**Availability:** 1991

**Second Source:** None

**Functions Contained:**

Memory controller supports conventional mode, page mode or 2-way page interleaving	Cache: No
Supports 512KB to 8MB DRAM	Clock Speed: 16 & 20 MHz
Supports shadow RAM of BIOS	Main Memory Support: Yes
Power down, sleep, & slow refresh	
8-bit/16-bit BIOS ROM select switch	Software configurable Wait States
Hardware/software selectable CPU speed	Fast GateA20 support
(2) compatible 8259 Interrupt controllers	Programmable synch/asynch expansion bus
(1) 75LS612 compatible memory mapper	Staggered refresh
	(2) compatible 8237 DMA controllers
	(1) 8254 compatible Timer/Counter

---



National Semiconductor PC87130

**Manufacturer:** National Semiconductor**Processor Supported:** 80286**System Bus:** XT, AT**Part:** PC87310, Dual UARTS with Floppy Disk Controller & High Perf. Parallel interface**Availability:** 1990**Second Source:** ?**Functions Contained:**

(2) UARTS (compatible with INS8250A, NS16450, &amp; NS16550AF)

Floppy Disk Controller (NEC mPD765A compatible)

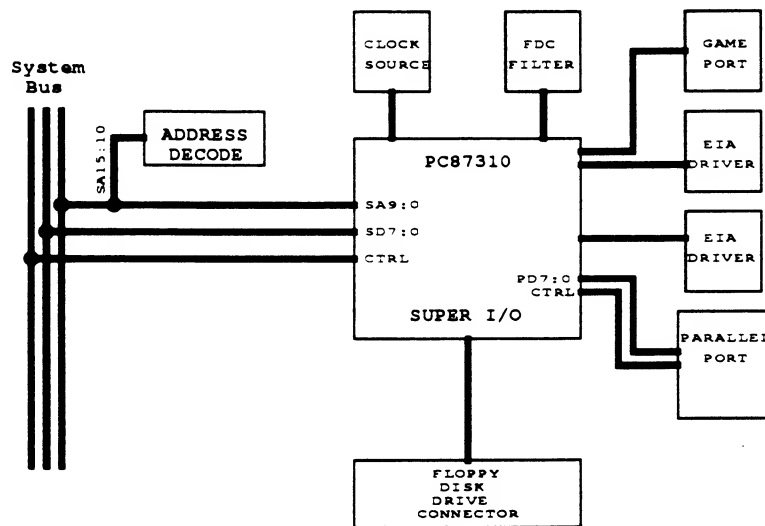
IDE Hard Disk Select Logic

**Cache:** No**Clock Speed:** 24 MHz Xtal**Main Memory Support:** No

Bi-directional Parallel Port

Game Port Select Logic

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National Semiconductor PC87310 Super I/O





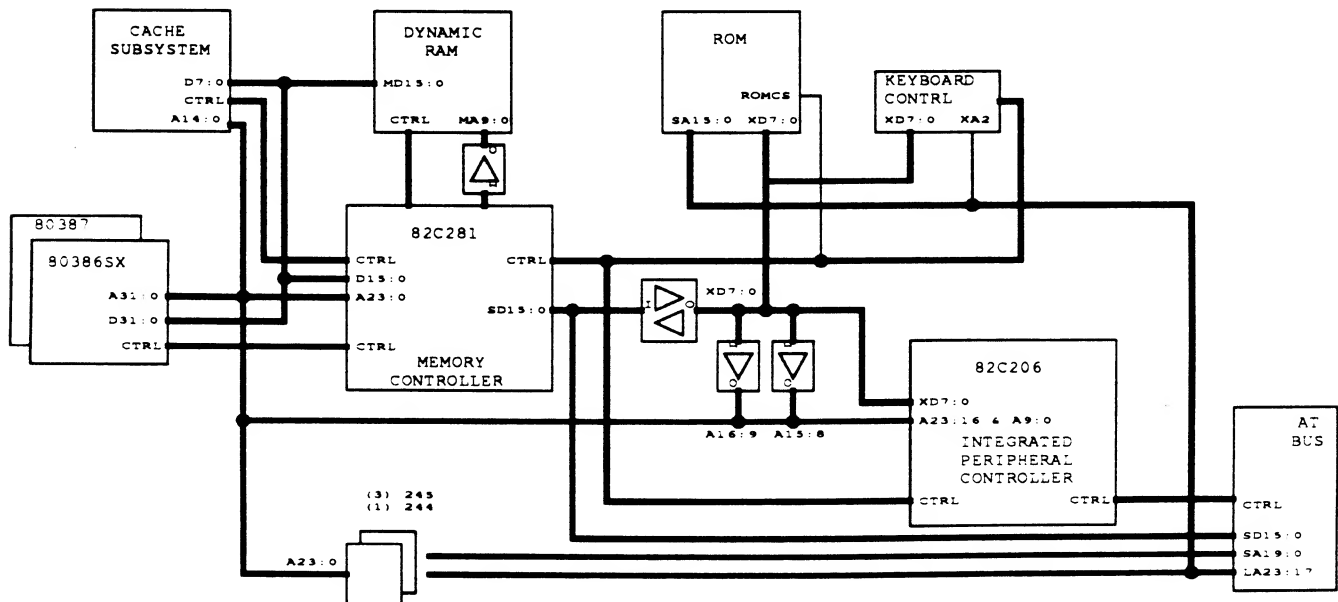
**Manufacturer:** Opti  
**Processor Supported:** 80386SX  
**System Bus:** AT  
**Part:** 82C281/2, Cache Sx/AT  
**Availability:** 1991  
**Second Source:** ?

**Cache:** Yes  
**Clock Speed:** 16, 20, & 25MHz  
**Main Memory Support:** Yes

**Functions Contained:**

DRAM control logic (1-16MB, with 256K, 1M & 4M devices)  
 Write through Cache Memory control  
 DMA/Refresh logic  
 Data bus control

Shadow RAM support  
 AT bus control logic  
 Programmable AT bus clock



OPTi 386 WB Cache using the 82C281 chip

\* CACHE SUBSYSTEM CONTAINS SRAM AND BUFFERS

## Personal Computer Design

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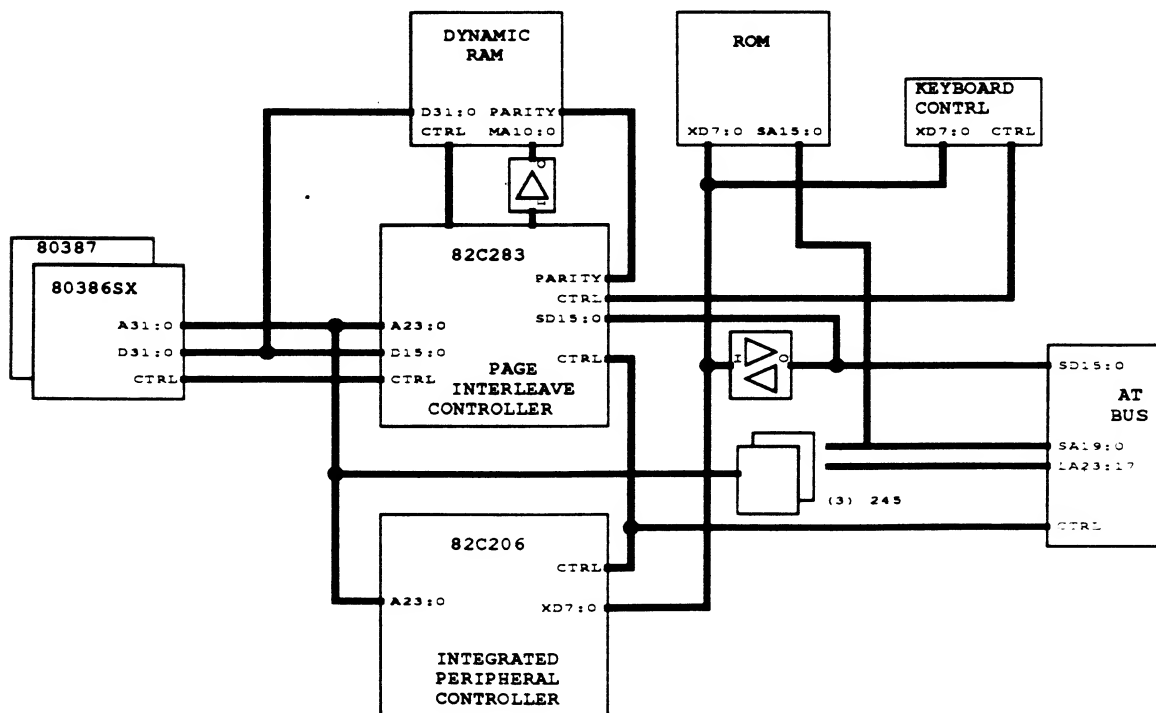
**Manufacturer:** Opti  
**Processor Supported:** 80386SX  
**System Bus:** AT  
**Part:** 82C283, Page Interleave Sx/At Controller  
**Availability:** Q1 1991  
**Second Source:** ?  
**Functions Contained:**

Page interleaved, local memory controller (1MB-16MB)  
AT Bus controller (DMA and Refresh logic)  
Data bus controller

**Cache:** No  
**Clock Speed:** 16, 20, & 25 MHz  
**Main Memory Support:** Yes

Shadow RAM logic  
Programmable AT bus clock  
Gate A20 support

---



OPTi 386SX Page Interleaved AT

**Manufacturer:** Opti

**Processor Supported:** 80386SX, Cyrix CX486SLC

**System Bus:** AT

**Part:** 82C291, CPU/CACHE/DRAM/AT Bus Controller (part of SXWB PC/AT Chipset)

**Availability:** Q3 1992

**Second Source:** none

**Functions Contained:**

Supports 4 banks of 256K, 1M, & 4M page-mode local DRAMs

Supports memory configurations up to 16MB

Write-back direct-mapped cache controller

Shadow RAM option

Supports 2 non-cacheable regions

Provides turbo/slow speed selection

Supports 0 or 1 wait state for 16-bit AT bus

Synchronous AT bus clock with programmable clock division options: CLK2/4,6,8,10

**Cache:** Yes

**Clock Speed:** 16 to 40 MHz

**Main Memory Support:** Yes

Supports flash ROM

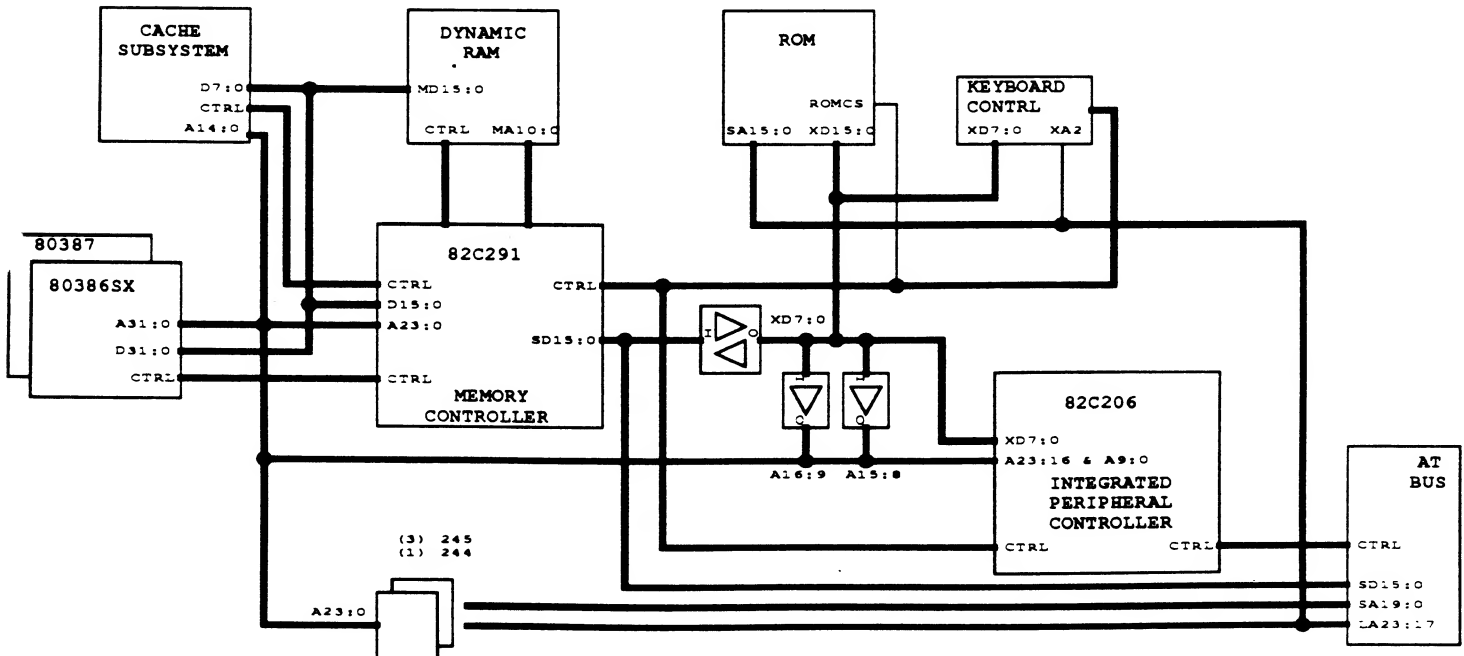
Supports programmable cache sizes: 16K, 32K, 64K, 128K

High performance Local Bus support

Hidden refresh, slow refresh & CAS before RAS refresh

Option for write protected, cacheable video BIOS

Supports fast CPU reset & GATEA20 generation



OPTi 386 WB Cache using the 82C291 chip

\* CACHE SUBSYSTEM CONTAINS  
SRAM AND BUFFERS

## Personal Computer Design

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**Manufacturer:** Opti

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** 82C381-25/33, High Integration, Direct Mapped Cache AT

**Availability:** 1989

**Second Source:** Chips & Tech. CS8230 based 82385 (Cache)

**Functions Contained:**

CPU interface & bus control

DMA/Master and DRAM Refresh logic

Reset/Shut Down logic

Numeric Processor Interface

Data buffers and latches

Cache controller logic

**Cache:** No

**Clock Speed:** 20, 25 or 33 MHz

**Main Memory Support:** Yes

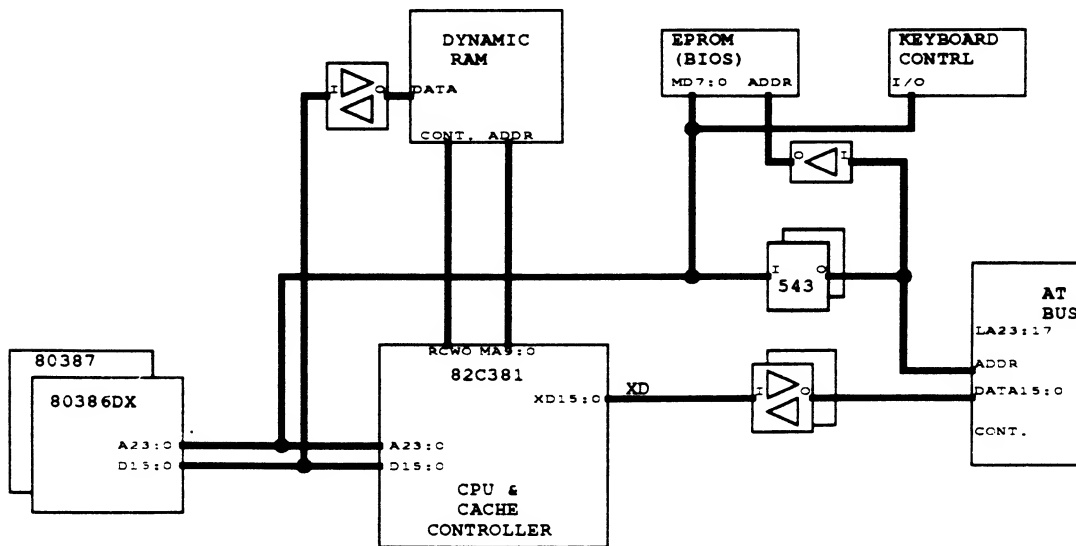
Programmable AT bus clock & CPU clock

Bus Arbitration logic

CPU/Bus State Machine

Data bus conversion & path control logic

Parity generation/detection



Opti 82C381 Cache

**Manufacturer:** Opti

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** 82C382D-25 -33, High Integration, Direct Mapped/Page Interleave Controller

**Availability:** 1989

**Second Source:** ? CS8230, 82385

**Functions Contained:**

Interfaces with Opti 82C381

DRAM and EPROM control logic

BIOS shadow RAM support

Gate A20 support

**Cache:** No

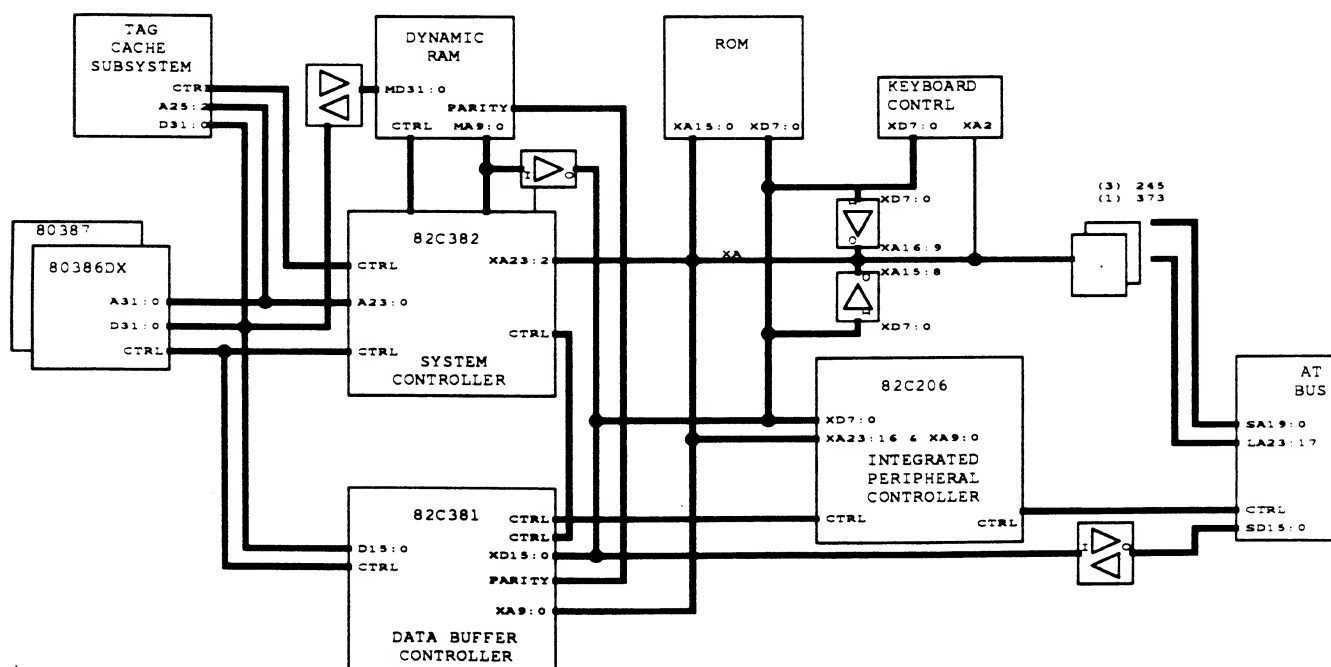
**Clock Speed:** 20, 25 or 33 MHz

**Main Memory Support:** Yes

32KB, 64KB, 128KB Direct Mapped Cache support

supports direct Mapped Cache interface

Relocation of top 256KB support



OPTi 386 Direct Mapped

\* CACHE SUBSYSTEM CONTAINS  
SRAM AND BUFFERS

## Personal Computer Design

**Manufacturer:** Opti

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** 82C391, System Controller (part of Opti-386WB AT Chipset)

**Availability:** Q1 1991

**Second Source:** ?

**Functions Contained:**

Write-back Cache controller (built in Tag comparator)

Reset Control for CPU and Numeric Processor

Burst Line Fill Control Logic

Shadow RAM logic

(2) Noncacheable Address Comparators

**Cache:** Yes

**Clock Speed:** 25, 33, & 40 MHz

**Main Memory Support:** Yes

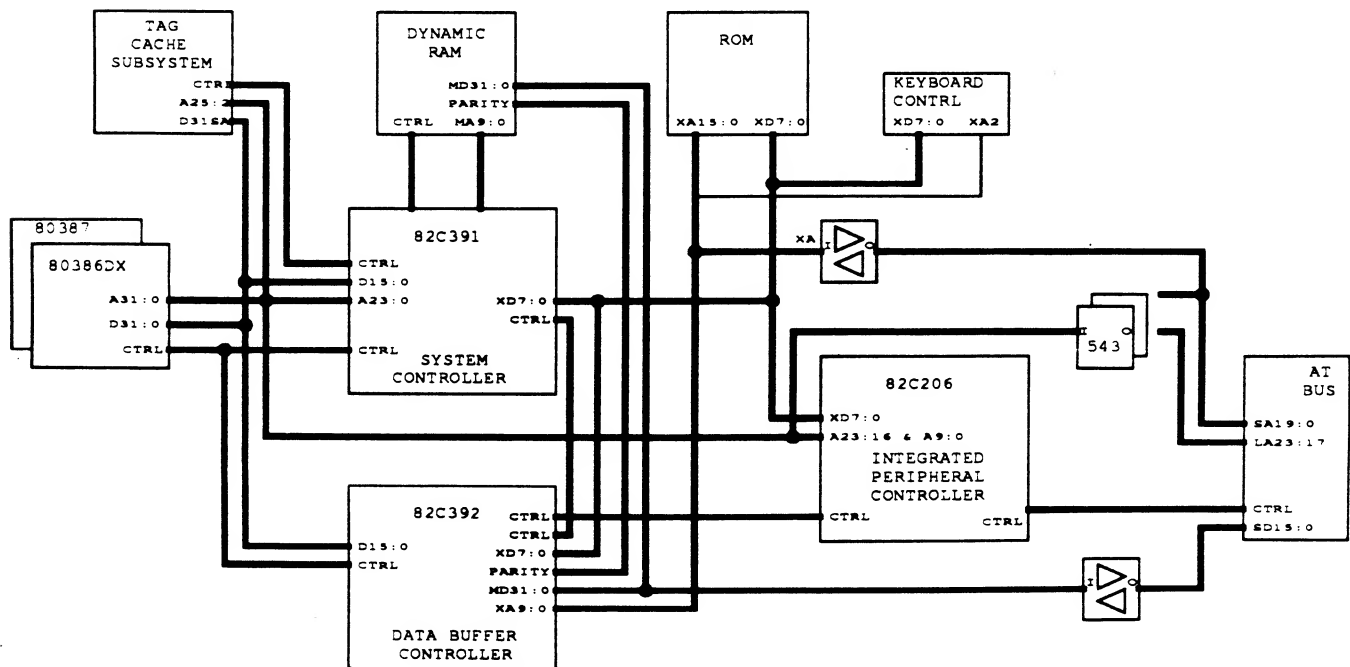
AT bus and CPU interface circuitry

Clock Generation (for CPU, Processor and AT bus)

Page Mode DRAM Controller

DMA and Refresh logic

(2) DMA upper address latches



OPTi 386 Write Back Cache

\* CACHE SUBSYSTEM CONTAINS  
SRAM AND BUFFERS

**Manufacturer:** Opti

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** 82C392, Data Buffer Controller (part of Opti-386WB AT Chipset)

**Availability:** Q1 1991

**Second Source:** ?

**Functions Contained:**

Data Bus conversion

AT bus direction

Clock source (for 80206 and 8042)

Speaker Control

Numerical Processor Interface

**Cache:** No

**Clock Speed:** 25, 33, & 40 MHz

**Main Memory Support:** No

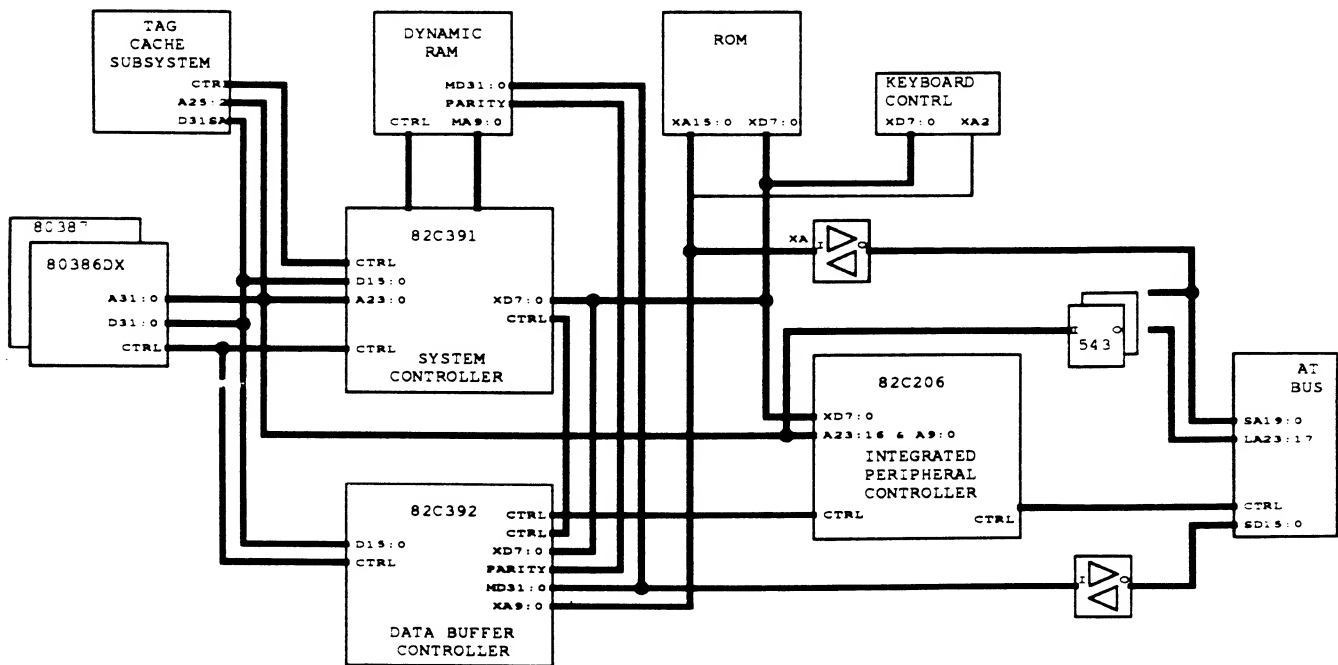
Parity Generation/Detection

Reset logic

Chip Select for Keyboard Controller and RTC

Port B, 70H and NMI Logic

Keyboard reset and Gate A20 emulation logic



OPTi 386 Write Back Cache

\* CACHE SUBSYSTEM CONTAINS SRAM AND BUFFERS

**Manufacturer:** Opti

**Processor Supported:** 80486

**System Bus:** AT

**Part:** 82C481-25/33, High Integration CPU Controller

**Availability:** 1989

**Second Source:** ?

**Functions Contained:**

CPU interface & bus control

DMA/Master and DRAM Refresh logic

Cache controller logic (direct-mapped)

Reset/Shut Down logic

Numeric Processor Interface

Data buffers and latches

**Cache:** No

**Clock Speed:** 25 or 33 MHz

**Main Memory Support:** Yes

Programmable AT bus clock & CPU clock

Port B register and NMI logic

Bus Arbitration logic

CPU/Bus State Machine

Data bus conversion & path control logic

Parity generation/detection

---

Schematic Not Available At Press Time



<b>Manufacturer:</b> Opti	<b>Cache:</b> No
<b>Processor Supported:</b> 80486	<b>Clock Speed:</b> 25 or 33 MHz
<b>System Bus:</b> AT	<b>Main Memory Support:</b> Yes
<b>Part:</b> 82C482-25/33, High Integration Burst Mode Cache/ Page Interleave Controller	
<b>Availability:</b> 1989	
<b>Second Source:</b> ?	
<b>Functions Contained:</b>	
DRAM and EPROM control logic	Shadow RAM and Memory Remapping
Cache Interface Logic	System Interface Logic
Configuration Registers	Address Latches

---

Schematic Not Available At Press Time

## Personal Computer Design

**Manufacturer:** Opti

**Processor Supported:** 80386, 80486

**System Bus:** AT

**Part:** 82C492, Data Buffer Controller (part of Opti-486WB AT Chipset)

**Availability:** Q1 1991

**Second Source:** ?

**Functions Contained:**

Data Bus conversion

AT bus direction

Clock source (for 80206 and 8042)

Speaker Control

Numerical Processor Interface (not used with 80486)

**Cache:** No

**Clock Speed:** 33, 40, & 50 MHz

**Main Memory Support:** No

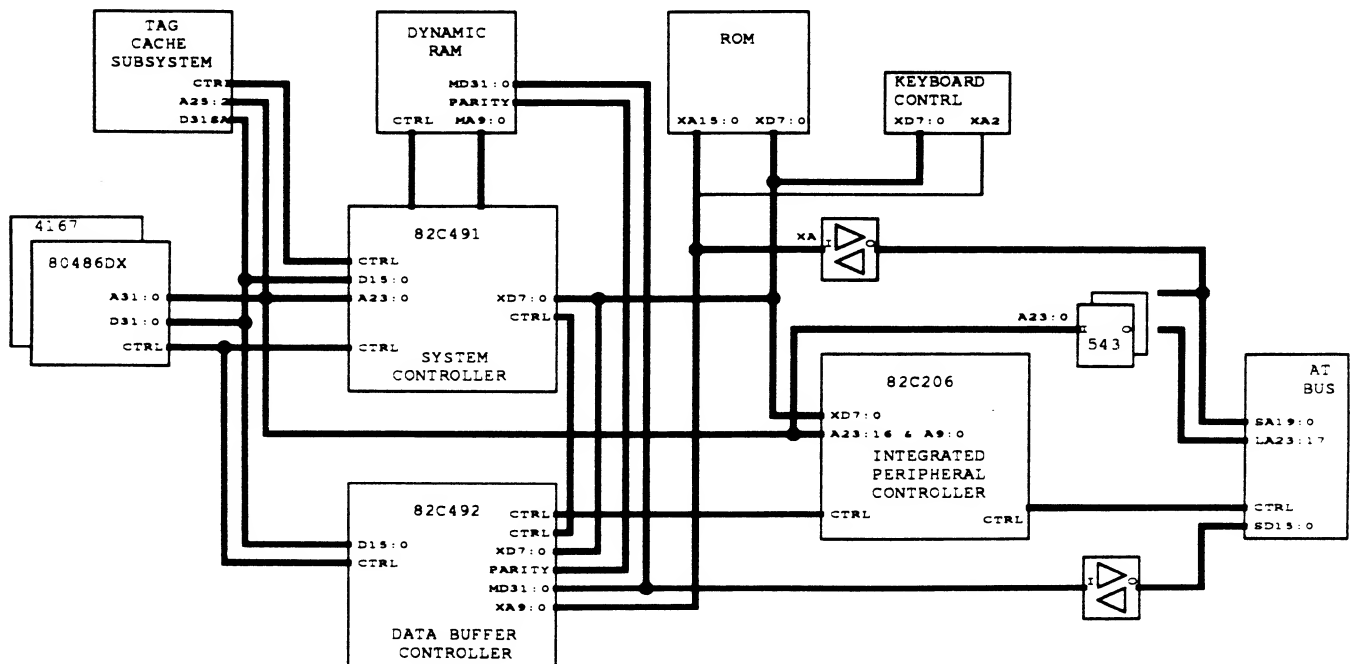
Parity Generation/Detection

Reset logic

Chip Select for Keyboard Controller and RTC

Port B, 70H and NMI Logic

Keyboard reset and Gate A20 emulation logic



OPTi 486 Write Back Cache

\* CACHE SUBSYSTEM CONTAINS  
SRAM AND BUFFERS

**Manufacturer:** Opti

**Processor Supported:** 80386, 80486

**System Bus:** AT

**Part:** 82C493, System Controller (part of Opti-486WB AT Chipset)

**Availability:** Q1 1991

**Second Source:** ?

**Functions Contained:**

Write-back Cache controller (built in Tag comparator)

AT bus and CPU interface circuitry

Clock Generation (for CPU, Processor and AT bus)

Burst line fill control logic

Shadow RAM logic

(2) DMA upper address latches

**Cache:** Yes

**Clock Speed:** 33, 40, & 50 MHz

**Main Memory Support:** Yes

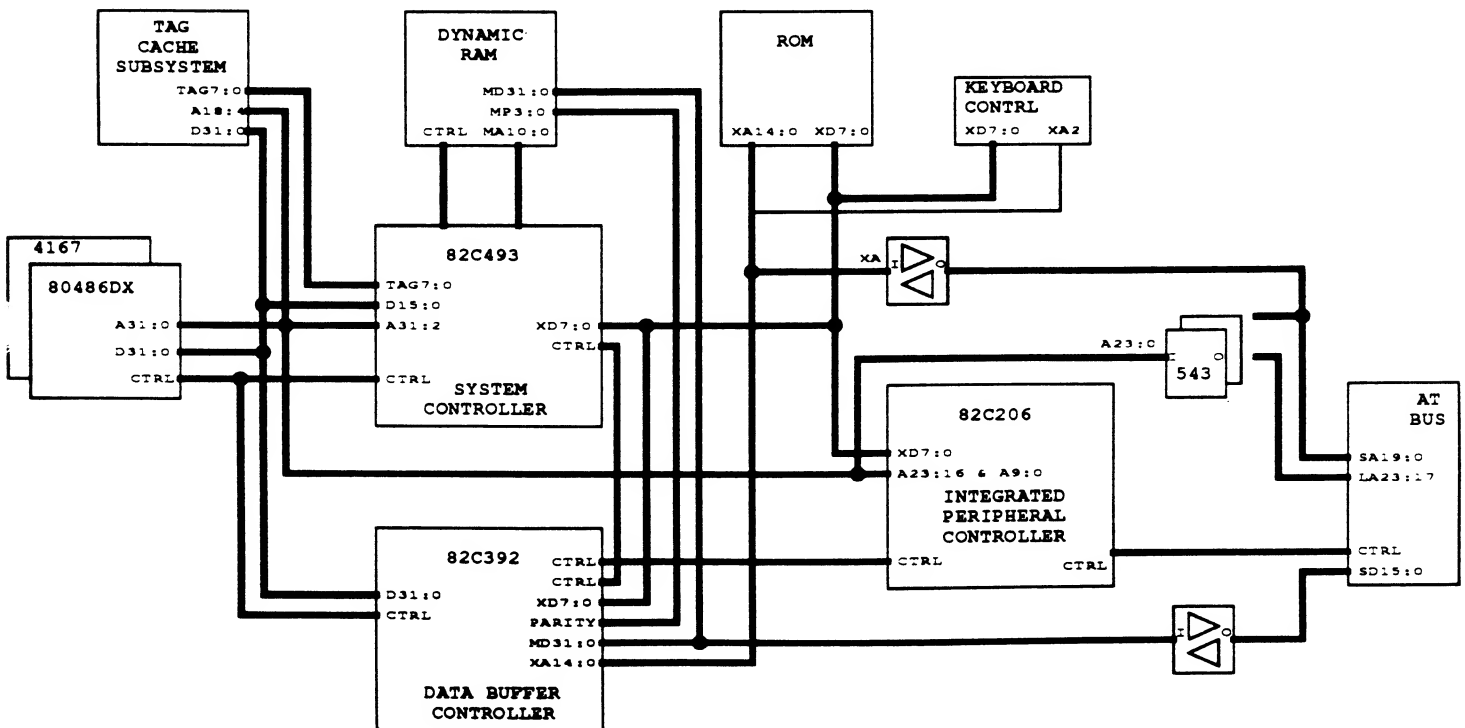
CPU internal cache control

Reset Control for CPU and Numeric Processor

CPU Burst mode control

Page Mode DRAM Controller

DMA and Refresh logic



OPTi 486 Write Back Cache: 82C493/82C392/82C206

\* CACHE SUBSYSTEM CONTAINS SRAM AND BUFFERS

## Personal Computer Design

**Manufacturer:** Opti

**Processor Supported:** 80386DX, 80486SX/DX

**System Bus:** AT

**Part:** 82C498, CPU/CACHE/DRAM/AT Bus Controller (part of DXWB PC/AT Chipset)

**Availability:** Q3 1992

**Second Source:** none

**Functions Contained:**

Write-back or write-through, direct-mapped, bank interleaved cache controller

Supports 4 banks of 256K, 1M, & 4M DRAMs

Supports 2 non-cacheable regions

Supports memory configurations up to 64 MB

Shadow RAM option

Hidden refresh, slow refresh & CAS before RAS refresh

Supports fast CPU reset & GATEA20 generation

Supports 2-1-1-1, 3-1-1-1, 2-2-2-2, & 3-2-2-2 cache burst cycles

Supports programmable cache sizes: 16K, 32K, 64K, 128K, 256K, & 512K

Synchronous AT bus clock with programmable clock division options: CLK2/4, 6, 8, 10

**Cache:** Yes

**Clock Speed:** up to 50 MHz

**Main Memory Support:** Yes

Supports 1X & 2X clock source

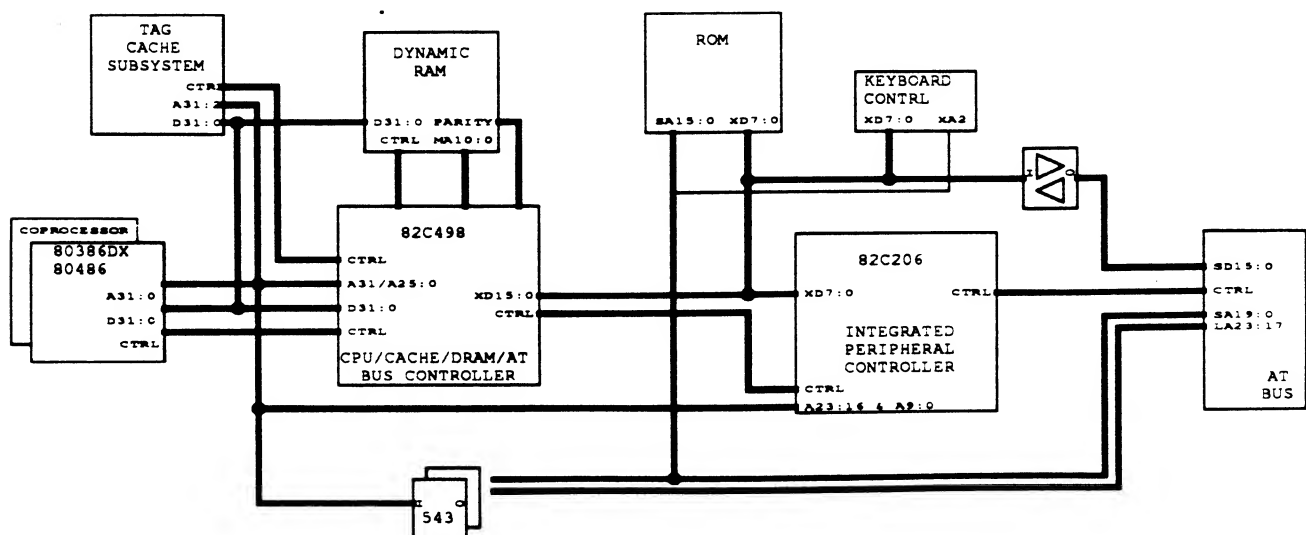
On-chip TAG auto-invalidation circuitry

Support 3-2-2-2 DRAM burst cycles

High performance Local Bus support

Provides turbo/slow speed selection

Supports 0 or 1 wait state for 16-bit AT bus



OPTi 498 CACHE

\* CACHE SUBSYSTEM CONTAINS SRAM AND BUFFERS

**Manufacturer:** PLX Technology

**Processor Supported:** 80386SX/DX, 80486, 80960

**System Bus:** AT, EISA, Micro Channel

**Part:** AT 9000, AT Bus Master Interface Chip

**Availability:** Q1 1991

**Second Source:** ?

**Functions Contained:**

Master control signal protocol converter (82596 to AT bus)

External buffer controller (enable, clocking and direction signals)

Programmable Data transfer rate (5 to 10 MBytes/second)

Slave controller

Address decoder (BIOS chip selects)

Clock generator

Hold Release Idle timer

**Cache:** No

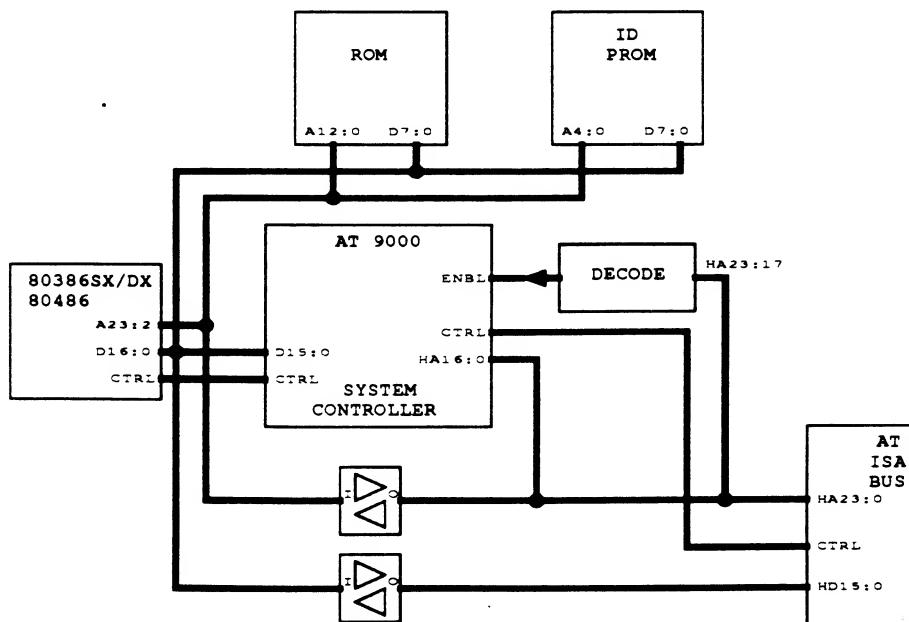
**Clock Speed:** up to 40 MHz

**Main Memory Support:** No

Bus arbitration

Interrupt generator (1 of 4 host interrupts)

Programmable configuration registers



PLX AT 9000 Bus Master Interface

## Personal Computer Design

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**Manufacturer:** PLX Technology

**Cache:** No

**Processor Supported:** 80386SX/DX, 80486, 80960

**Clock Speed:** up to 40 MHz

**System Bus:** AT, EISA, Micro Channel

**Main Memory Support:** No

**Part:** AT 9010, AT (ISA) Bus Master Interface Chip (for National DP83932)

**Availability:** Q1 1991

**Second Source:** ?

**Functions Contained:**

Master control signal protocol converter (local to Micro Channel)

Address decoder (memory and I/O chip selects)

Interrupt generator (1 of 4 host interrupts)

External buffer controller (enable, clocking and direction signals)

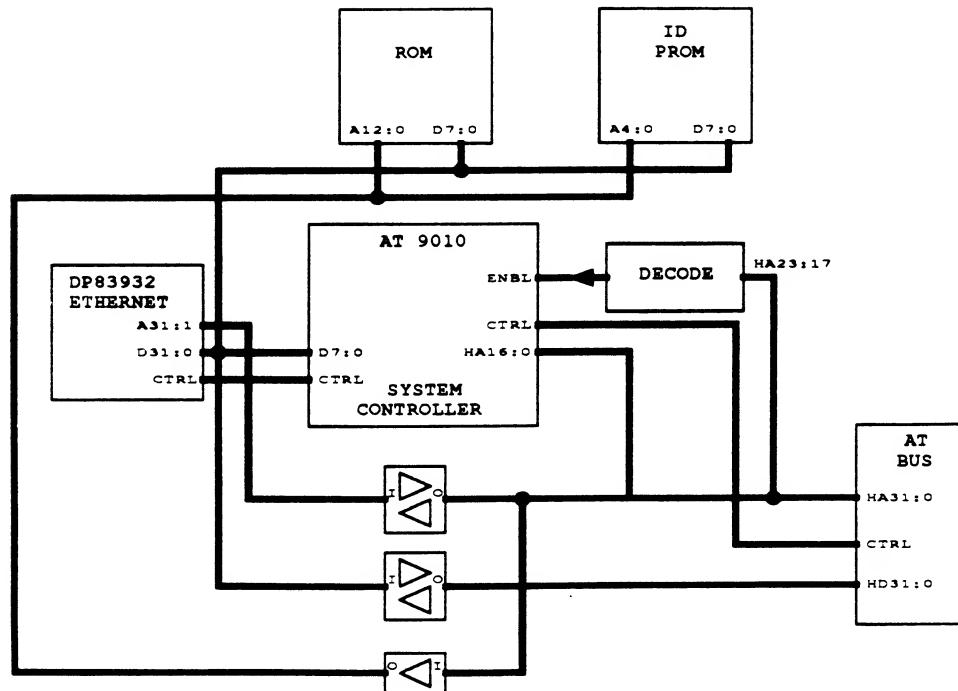
Slave controller

Bus arbitration

Clock generator

Programmable configuration registers

---



PLX AT 9010 Bus Master Interface  
for National DP83932 Ethernet Controller

**Manufacturer:** PLX Technology

**Cache:** No

**Processor Supported:** 80386SX/DX, 80486, 80960

**Clock Speed:** up to 40 MHz

**System Bus:** AT, EISA, Micro Channel

**Main Memory Support:** No

**Part:** AT 9020, AT (ISA) Bus Master Interface Chip (for Intel 82596)

**Availability:** Q1 1991

**Second Source:** ?

**Functions Contained:**

Master control signal protocol converter (local to Micro Channel)

Address decoder (memory and I/O chip selects)

Interrupt generator (1 of 4 host interrupts)

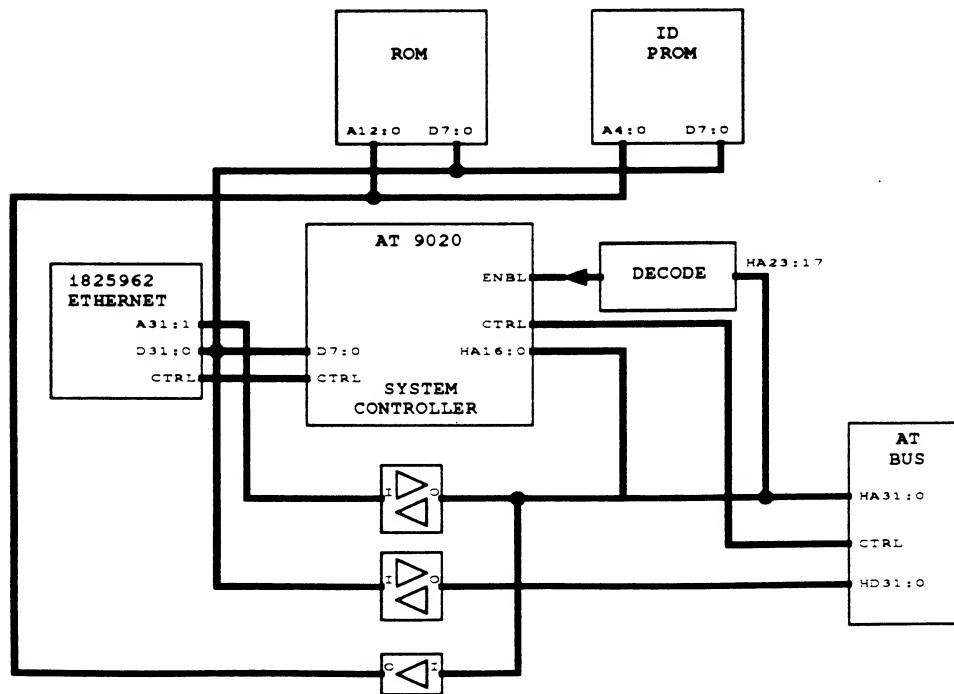
External buffer controller (enable, clocking and direction signals)

Slave controller

Bus arbitration

Clock generator

Programmable configuration registers



PLX AT 9020 Bus Master Interface  
for Intel 82596 Ethernet Controller

**Manufacturer:** PLX Technology

**Cache:** No

**Processor Supported:** 80386SX/DX, 80486, 80960

**Clock Speed:** up to 33 MHz

**System Bus:** AT, EISA, Micro Channel

**Main Memory Support:** No

**Part:** AT 9020 BV, EISA Bus Master Interface Chip (for Intel 82596)

**Availability:** Q1 1992

**Second Source:** ?

**Functions Contained:**

Converts all handshakes from local to EISA signals

Provides slave interface for control of adapter boards

Supports EISA Burst Mode Data rates to 33 MB/sec

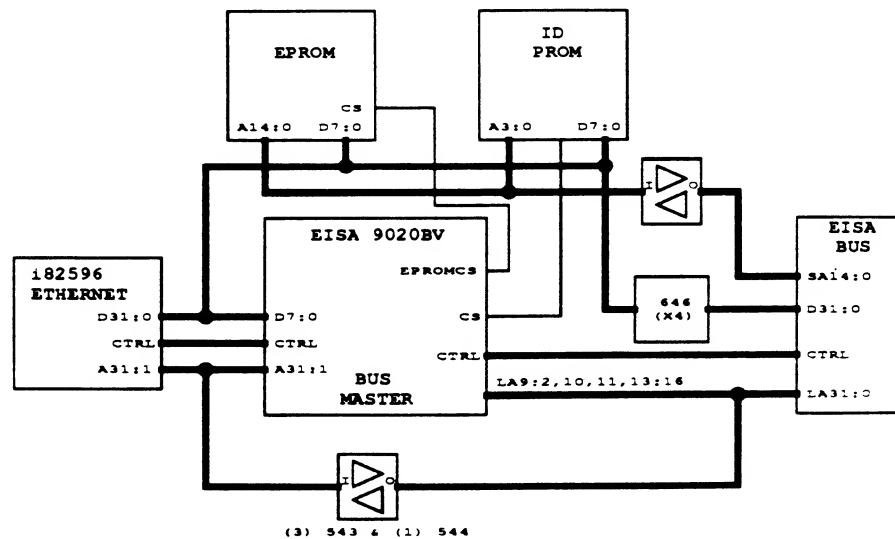
BIOS PROM and Node ID PROM support

Direct connect to System Bus of all Host Interface Control Signals

Generates 1 of 4 host interrupts from local interrupt

All signals drive EISA bus directly

---



PLX EISA 9020BV EISA Bus Master Interface Chip  
for Intel 82596 LAN Controller



**Manufacturer:** PLX Technology

**Processor Supported:** 80386SX/DX, 80486, 80960

**System Bus:** Micro Channel

**Part:** MC9000, Bus Master Interface Chip

**Availability:** Dec 1990

**Second Source:** ?

**Functions Contained:**

Master control signal protocol converter (local to Micro Channel)

Slave controller

Bus arbitration

Address decoder (ROM and I/O chip selects)

Interrupt generator (1 of 4 host interrupts)

External buffer controller (enable, clocking and direction signals)

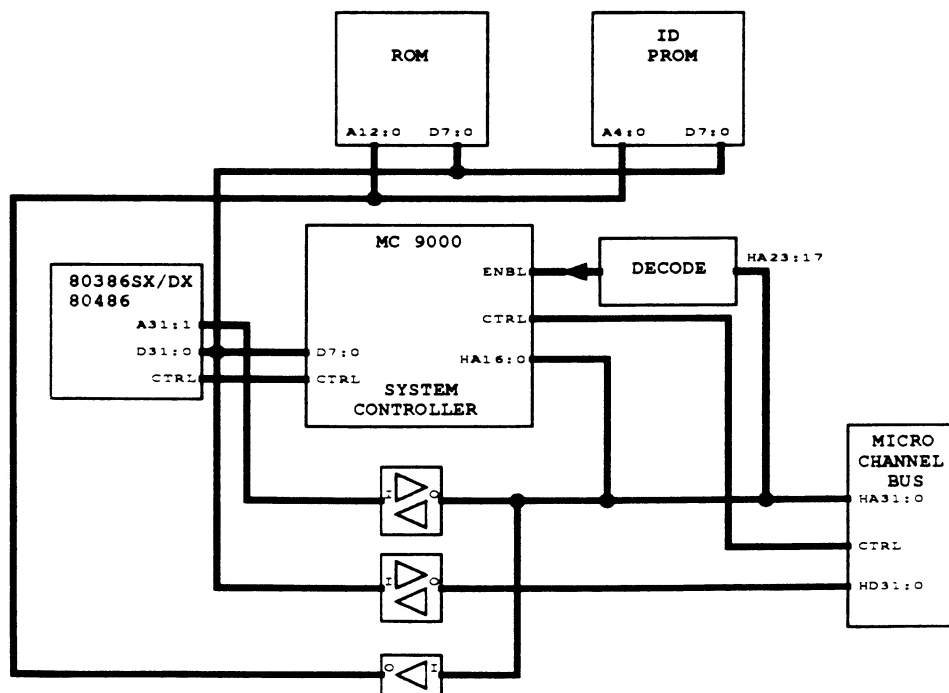
Clock generator

Programmable configuration registers

**Cache:** No

**Clock Speed:** up to 40 MHz

**Main Memory Support:** No



PLX MC 9000 Bus Master Interface

## Personal Computer Design

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**Manufacturer:** PLX Technology

**Processor Supported:** 80386SX/DX, 80486, 80960

**System Bus:** AT, EISA, Micro Channel

**Part:** MCA 1200/1210, Micro Channel Controller and Local Arbiter

**Availability:** 1989

**Second Source:** ?

**Functions Contained:**

Micro Channel Master bus controller

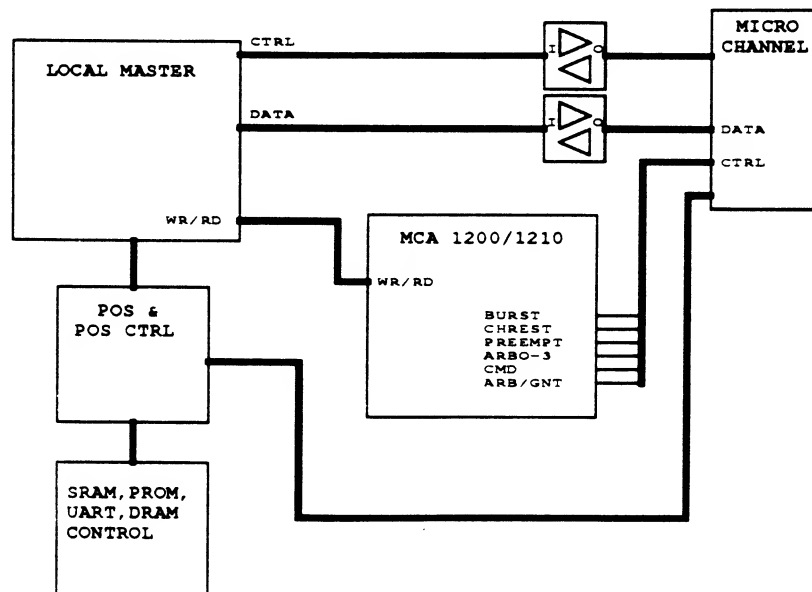
Local arbitration (fairness option)

1200 supports levels 12-15

1210 supports levels 8-11

Burst or single cycle data transfer support

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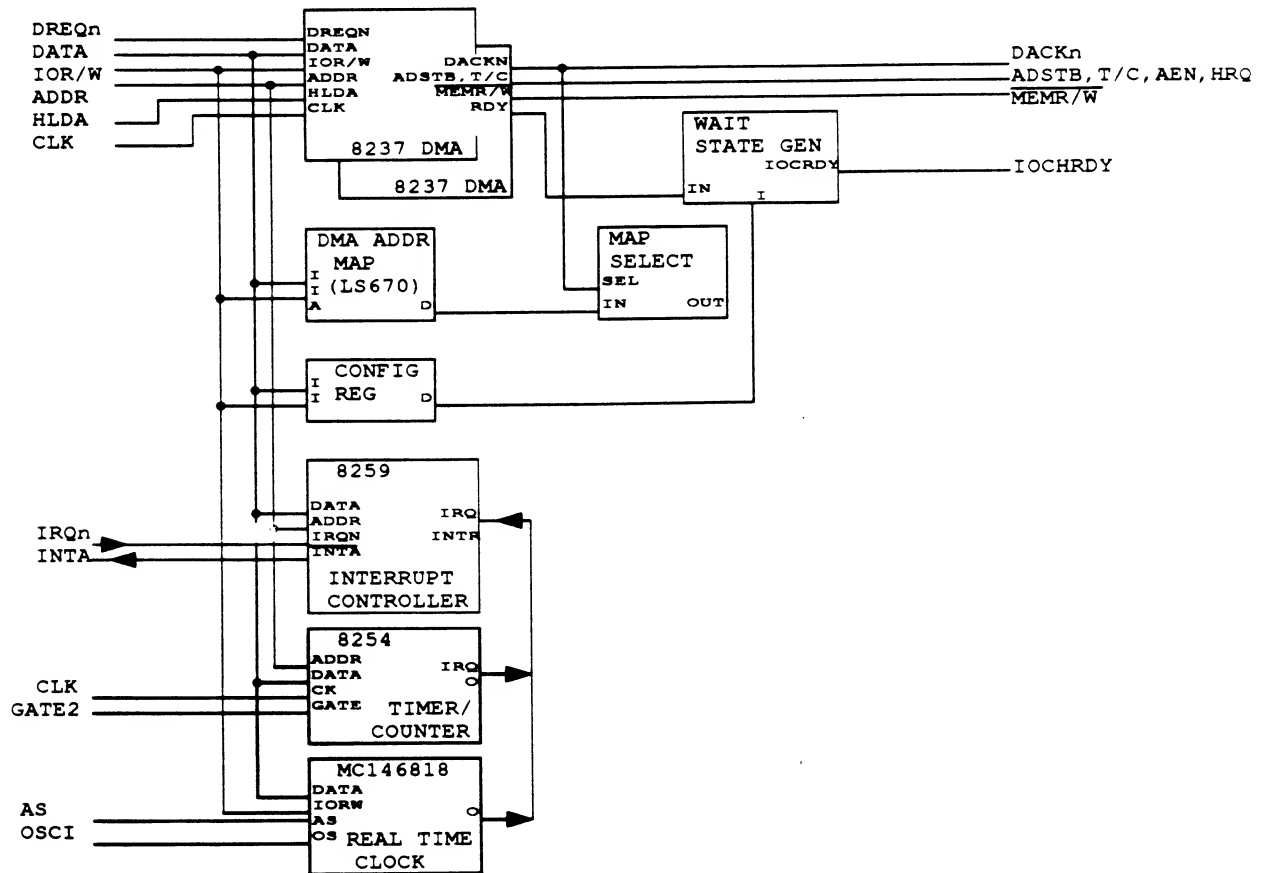
PLX MCA 1200/1210 Bus Controller & Local Arbiter

**Manufacturer:** Siemens Components, Inc.  
**Processor Supported:** 80386SX/DX, 80486, 80960  
**System Bus:** XT, AT  
**Part:** SAB 82C206, Integrated Peripheral Controller  
**Availability:** Q1 1989  
**Second Source:** ?

**Cache:** No  
**Clock Speed:** ? MHz  
**Main Memory Support:** No

**Functions Contained:**

(2) 8237 DMA Controllers (7 DMA channels)	(2) 8259 Interrupt controllers (13 request channels)
(1) 8254 timer/counter (2 channels)	(1) 146818 real time clock
(1) 74LS612 memory mapper	114 Bytes of CMOS RAM
Programmable wait states (DMA cycle and internal access)	



82206 Integrated Peripheral Controller

**Manufacturer:** Sun Electronics Corp  
**Processor Supported:** 80286, 80386SX  
**System Bus:** XT, AT  
**Part:** ST62C251-A, Bus Memory Controller (part of SUNTAC ST62C25 Chip Set)  
**Availability:** ?

**Cache:** No  
**Clock Speed:** 16 or 20 MHz  
**Main Memory Support:** Yes

**Second Source:** ?

**Functions Contained:**

Address mapper/decoder circuit (up to 8MB DRAM, 128 KB ROM)

AT bus controller (6 or 8 MHz)

8-bit/16-bit PROM access

Data bus control circuit

4 way page interleave memory support

Shadow RAM support

Clock select circuit

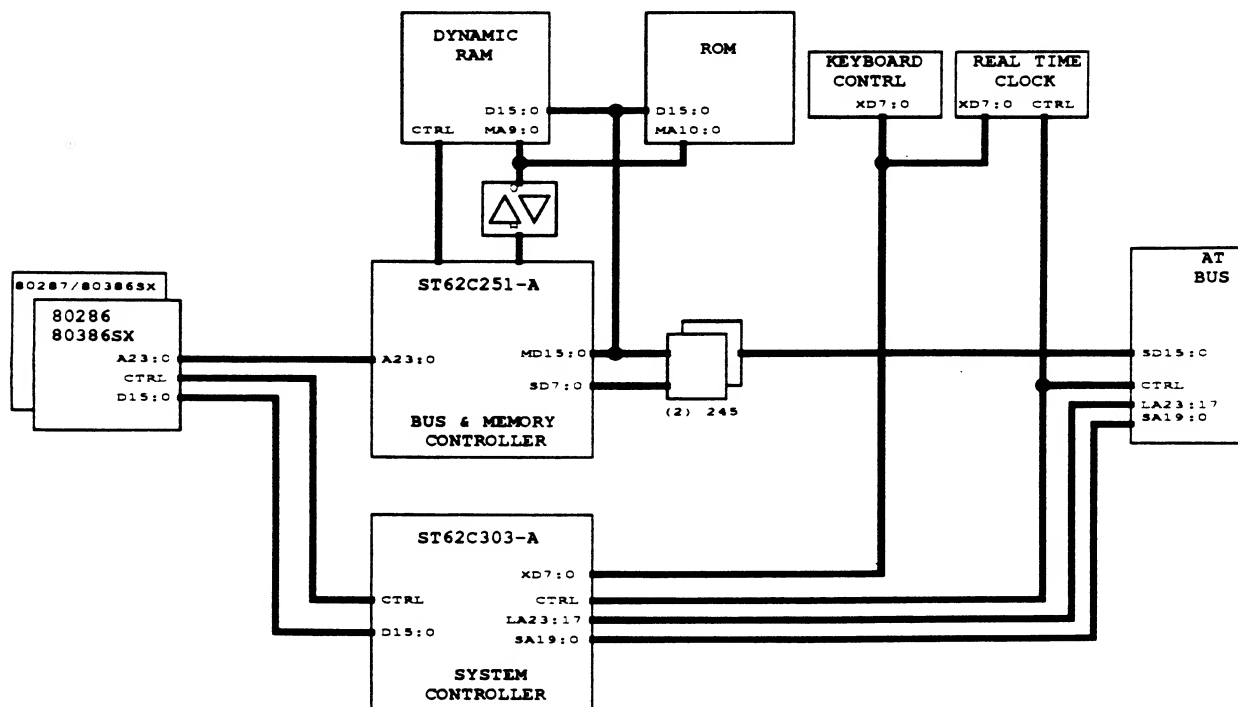
System memory control circuit

8-bit/16-bit conversion circuit (for AT bus)

Programmable wait state logic

Quick gate A20 control

Staggered Refresh logic (AT bus and DRAM)



Sun Electronics SUNTAC ST62C25 Chip Set

**Manufacturer:** Sun Electronics Corp  
**Processor Supported:** 80286, 80386SX  
**System Bus:** XT, AT

**Part:** ST62C303-A, SIO: System I/O Controller (part of SUNTAC ST62C25 Chip Set)

**Availability:** ?

**Second Source:** ?

**Functions Contained:**

(2) 82C37 DMA controllers

(1) 82C54 Timer Counter

AT bus command drive control circuit

DMA upper and lower address latch circuits

I/O address decoder circuit

NMI register circuit

Refresh counter circuit

**Cache:** No

**Clock Speed:** 16 or 20 MHz

**Main Memory Support:** Yes

(2) 82C59 Interrupt Controllers

Address bus latch/ bus driver control circuits

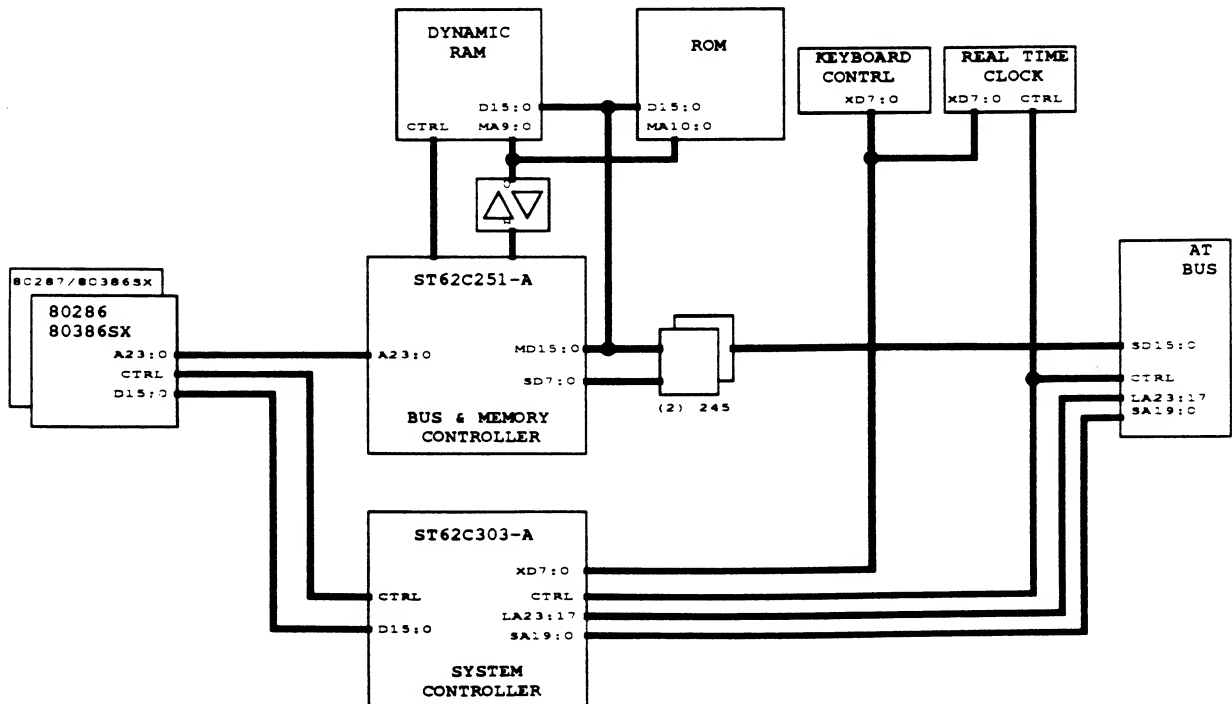
DMA page address register circuit

DMA Ready circuit

B-port circuit

Co-processor control circuit

Video clock oscillator circuit (14.31818 MHz)



Sun Electronics SUNTAC ST62C25 Chip Set

**Manufacturer:** Sun Electronics Corp

**Processor Supported:** 80286

**System Bus:** XT, AT

**Part:** ST62C241-A, Bus Memory Controller (part of SUNTAC ST62C24 Chip Set)

**Availability:** ?

**Second Source:** ?

**Functions Contained:**

Address mapper/decoder circuit (up to 8MB DRAM, 128 KB ROM)

AT bus controller (6 or 8 MHz)

8-bit/16-bit PROM access

Data bus control circuit

4 way page interleave memory support

Quick gate A20 control

Staggered Refresh logic (AT bus and DRAM)

**Cache:** No

**Clock Speed:** 12.5 MHz

**Main Memory Support:** Yes

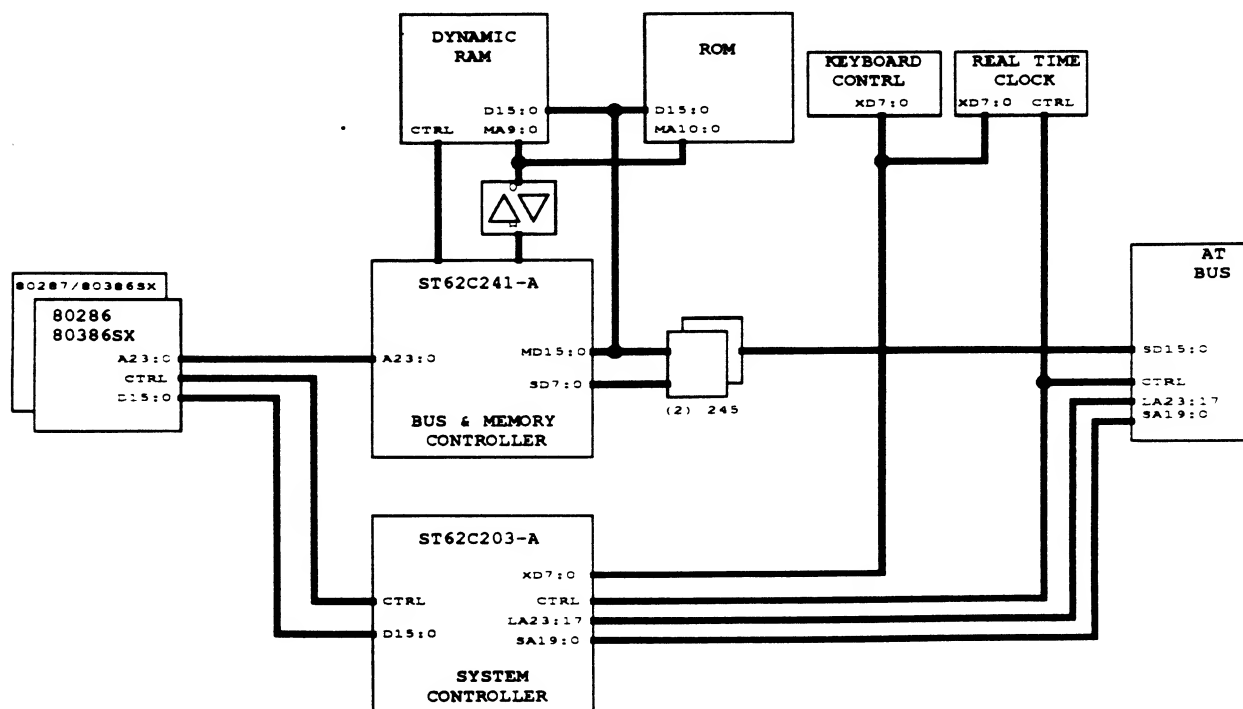
System memory control circuit

8-bit/16-bit conversion circuit (for AT bus)

Programmable wait state logic

Shadow RAM support

Clock select circuit



Sun Electronics SUNTAC ST62C24 Chip Set

**Manufacturer:** Sun Electronics Corp

**Processor Supported:** 80286

**System Bus:** XT, AT

**Part:** ST62C203-A, SIO: System I/O Controller (part of SUNTAC ST62C24 Chip Set)

**Availability:** ?

**Second Source:** ?

**Functions Contained:**

(2) 82C37 DMA controllers

(1) 82C54 Timer Counter

AT bus command drive control circuit

DMA upper and lower address latch circuits

I/O address decoder circuit

NMI register circuit

Refresh counter circuit

**Cache:** No

**Clock Speed:** 16 or 20 MHz

**Main Memory Support:** No

(2) 82C59 Interrupt Controllers

Address bus latch/ bus driver control circuits

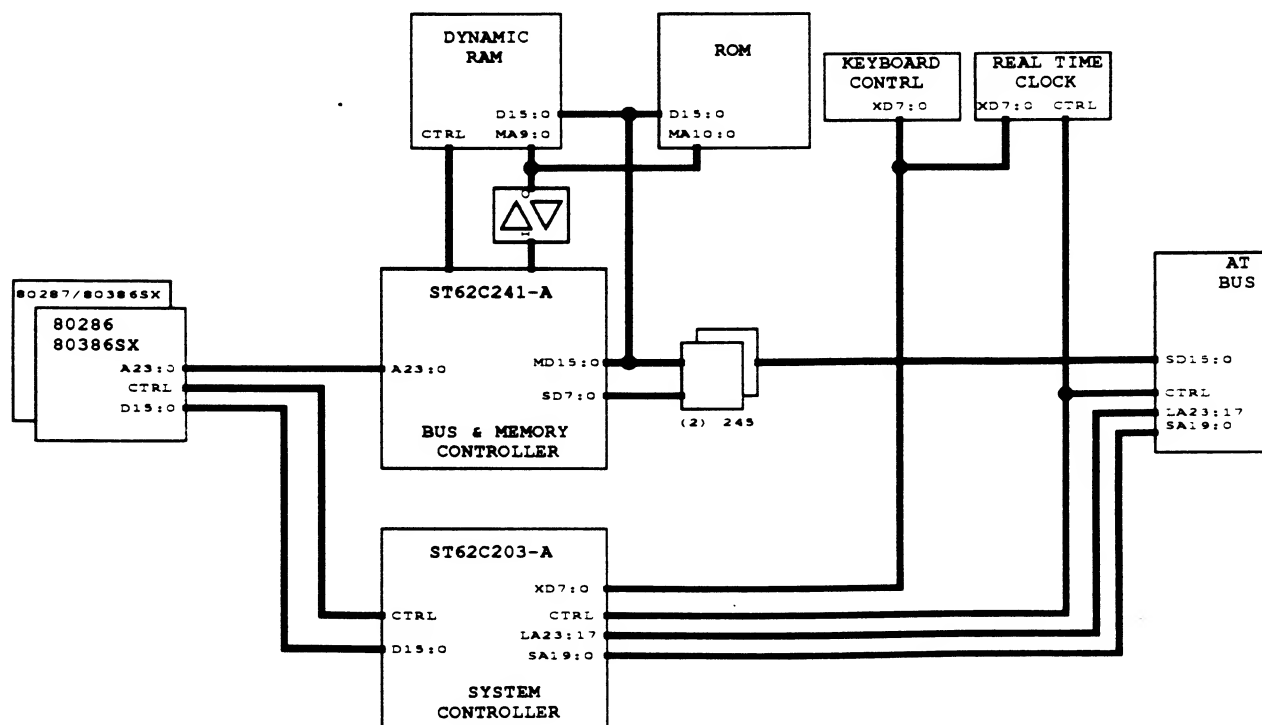
DMA page address register circuit

DMA Ready circuit

B-port circuit

Co-processor control circuit

Video clock oscillator circuit (14.31818 MHz)



Sun Electronics SUNTAC ST62C24 Chip Set

**Manufacturer:** Symphony Labs  
**Processor Supported:** 80386DX  
**System Bus:** AT

**Cache:** Yes  
**Clock Speed:** 25, 33, & 40 MHz  
**Main Memory Support:** Yes

**Part:** SL82C361, System Controller (part of SL82C360 386DX Chip Set)

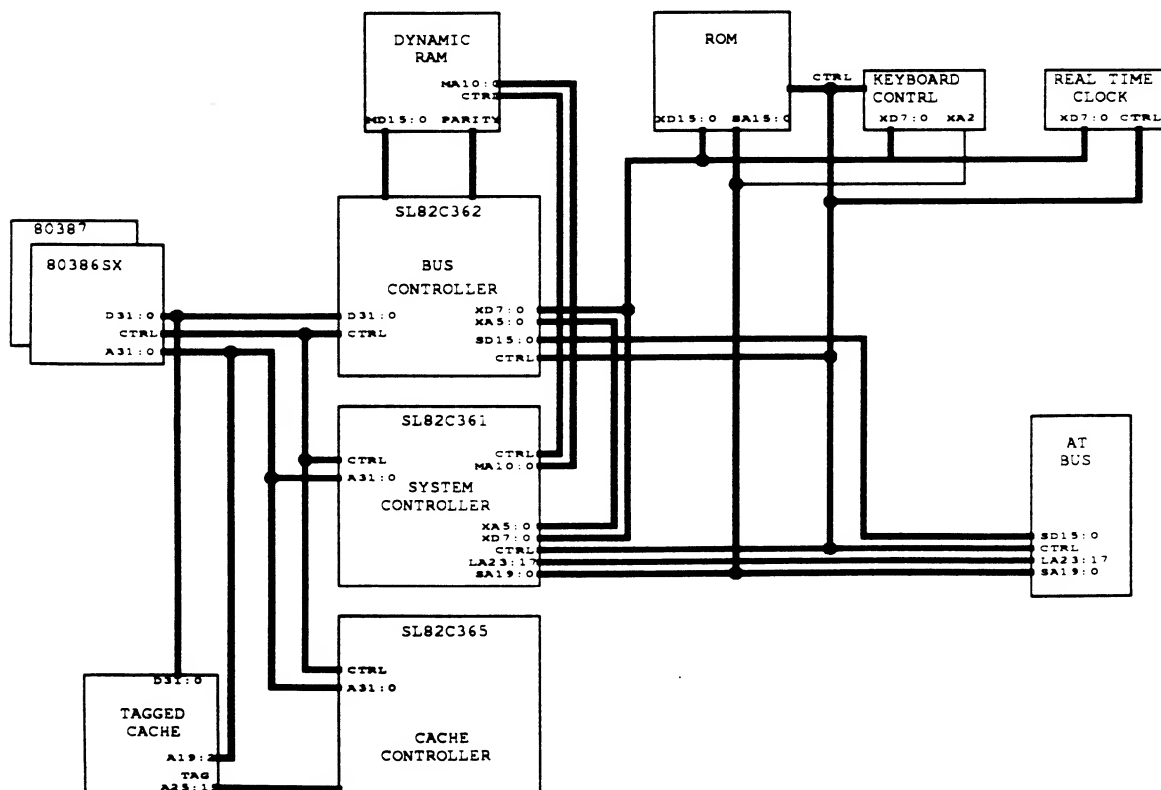
**Availability:** ?

**Second Source:**

**Functions Contained:**

System control signals for 80486 interface  
Page and 2/4 way page interleave  
Shadow ROM (16K increments)  
Supports 8-bit EPROMS  
Decoders for cache flushes

Non-cacheable region and memory relocation support  
Addressing for 1 to 4 banks of DRAM (up to 64MB)  
Programmable timing  
A20 gate support  
Supports synchronous and asynchronous AT bus operations



Symphony Labs SL82C360 386DX Chipset



**Manufacturer:** Symphony Labs

**Processor Supported:** 80486

**System Bus:** AT

**Part:** SL82C362, SBus Controller (part of SL82C460 Chip Set)

**Availability:** ?

**Second Source:**

**Functions Contained:**

Provides bus interface for CPU data bus (D), memory bus (MD), system bus (SD) and peripherals bus (XD)

(two) 8237 compatible DMA Controllers

(two) 8259A compatible Interrupt Controllers

(one) 8254 compatible timer/counter

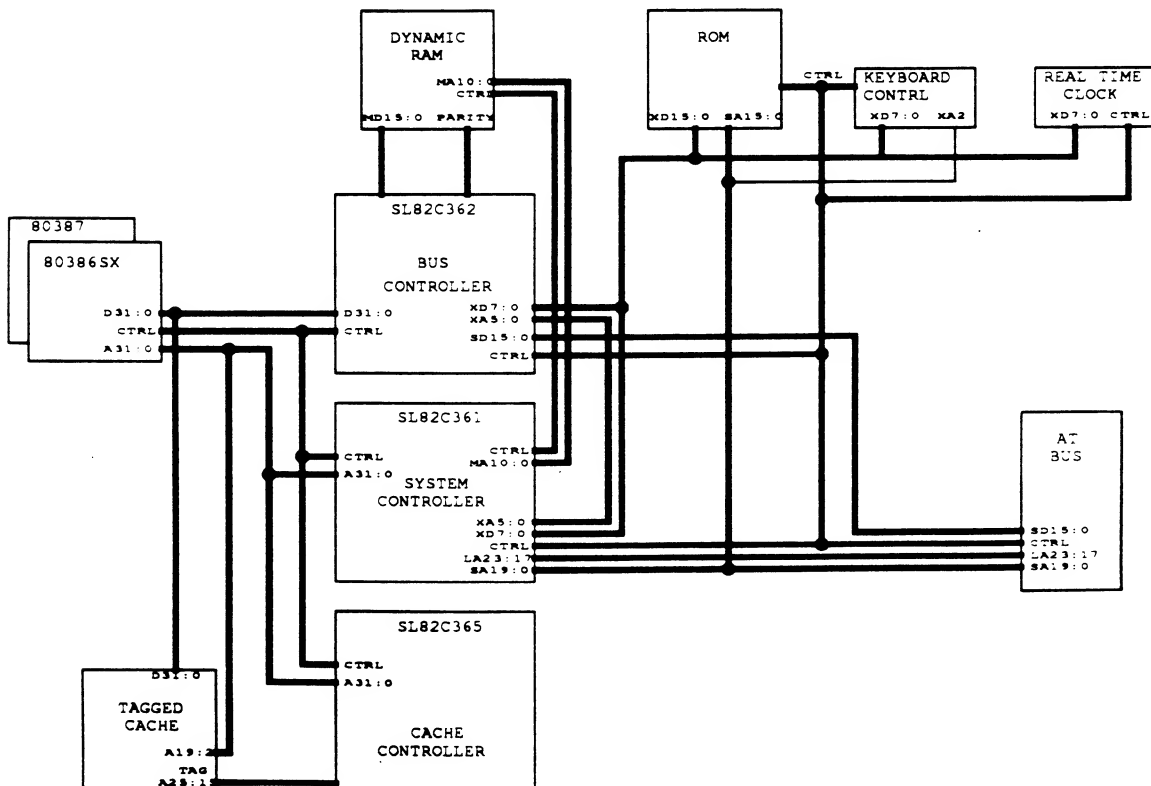
Port B and NMI logic

Parity generation/detection

**Cache:** Yes

**Clock Speed:** 25, 33, 40 & 50 MHz

**Main Memory Support:** Yes



Symphony Labs SL82C360 386DX Chipset

**Manufacturer:** Symphony Labs

**Processor Supported:** 80486

**System Bus:** AT

**Part:** SL82C362, System Controller (part of SL82C460 Chip Set)

**Availability:** ?

**Second Source:**

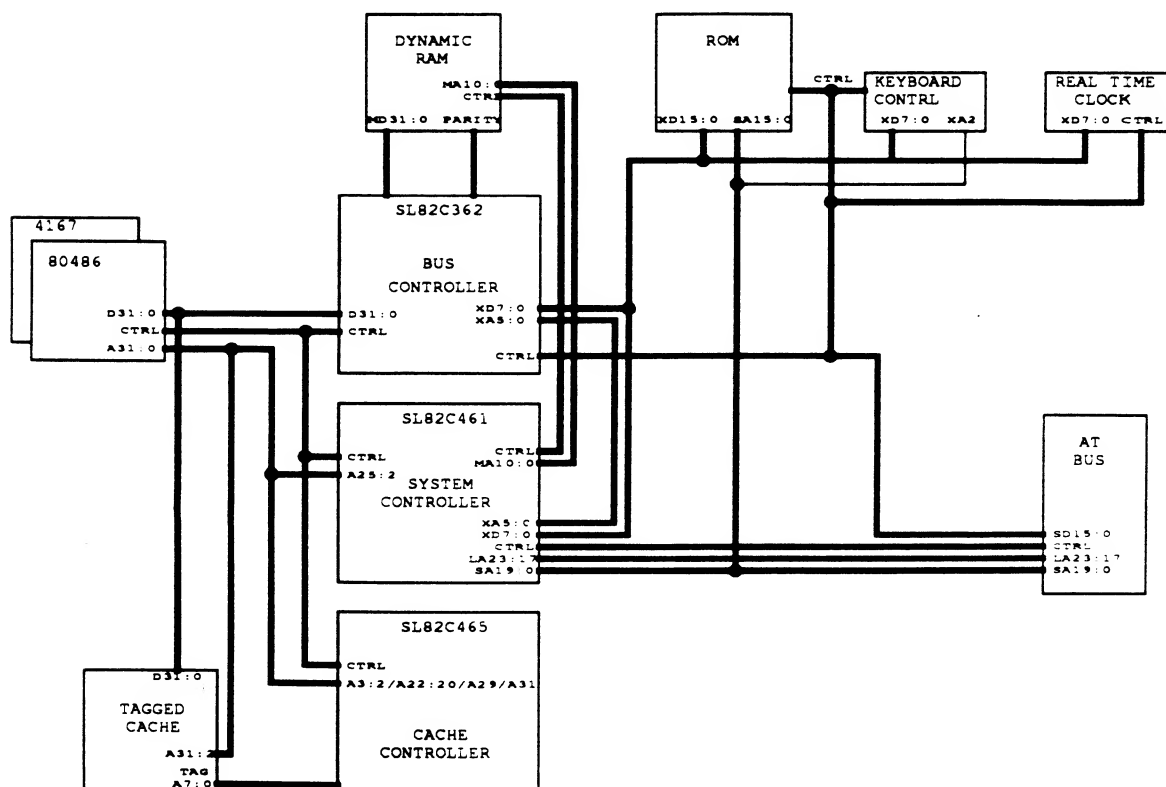
**Functions Contained:**

Provides bus interface for CPU data bus (D), memory bus (MD), system bus (SD and peripherals bus (XD)  
(two) 8237 compatible DMA Controllers

**Cache:** Yes

**Clock Speed:** 25, 33, 40 & 50 MHz

**Main Memory Support:** Yes

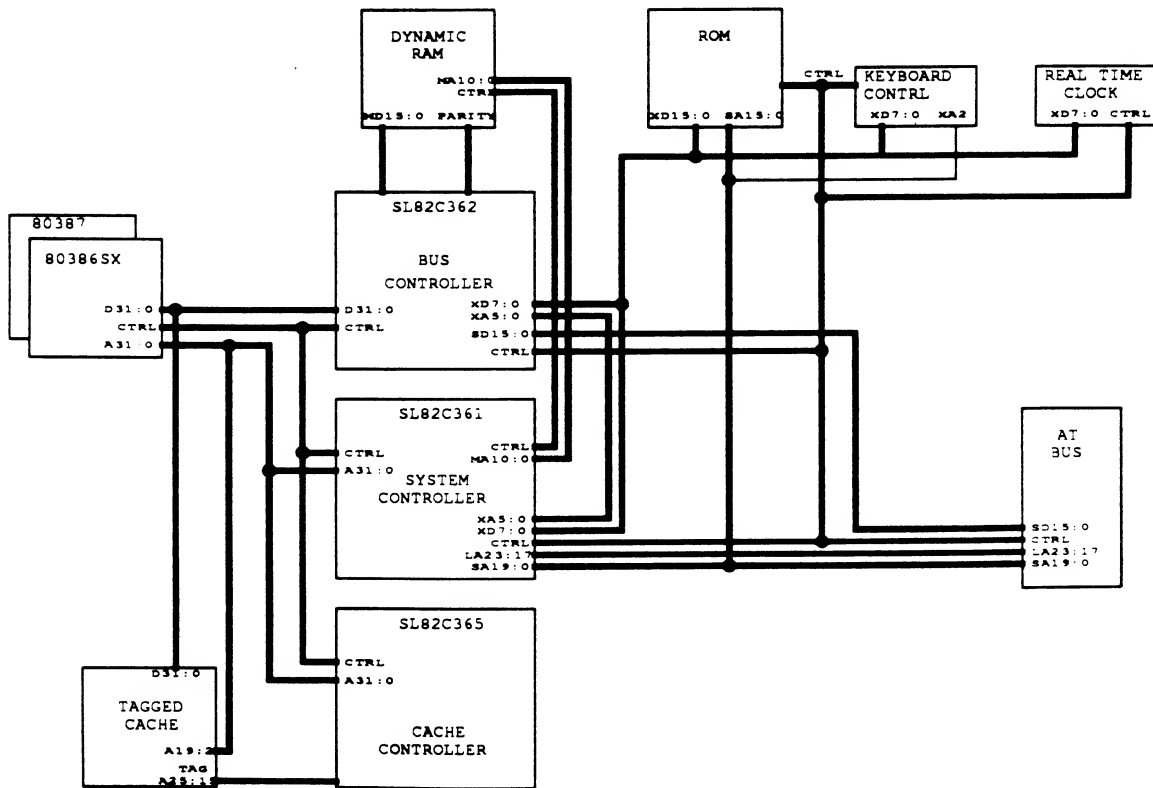


Symphony Labs SL82C460 486 Chipset

**Manufacturer:** Symphony Labs  
**Processor Supported:** 80386SX/DX  
**System Bus:** AT  
**Part:** SL82C365, 386 Cache Controller  
**Availability:** since 1991  
**Second Source:** none  
**Functions Contained:**  
Supports 16KB to 1MB cache size (1 to 4 double words)  
Tag comparison and posted write control  
80387 / WT3167 interface

**Cache:** Yes  
**Clock Speed:** 25, 33, & 40 MHz  
**Main Memory Support:** No

Burst mode cache fill  
Non-cacheable region support



Symphony Labs SL82C360 386DX Chipset

**Manufacturer:** Symphony Labs

**Processor Supported:** 80486

**System Bus:** AT

**Part:** SL82C461, System Controller (part of SL82C460 Chip Set)

**Availability:** ?

**Second Source:**

**Functions Contained:**

System control signals for 80486 interface

Addressing for 1 to 4 banks of DRAM (up to 64MB)

Shadow ROM (16K increments)

Supports 8-bit EPROMS

**Cache:** Yes

**Clock Speed:** 25, 33, 40 & 50 MHz

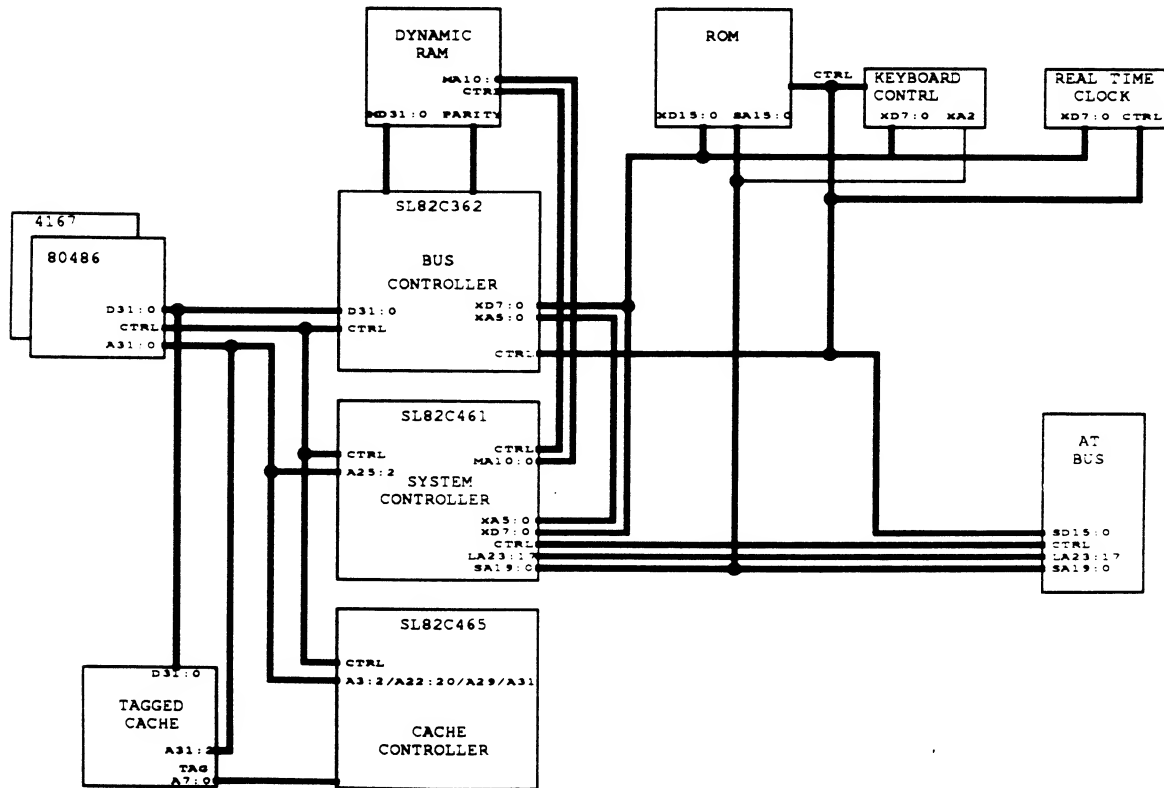
**Main Memory Support:** Yes

Non-cacheable region and memory relocation support

Page and 2/4 way page interleave

Programmable timing

A20 gate support



Symphony Labs SL82C460 486 Chipset

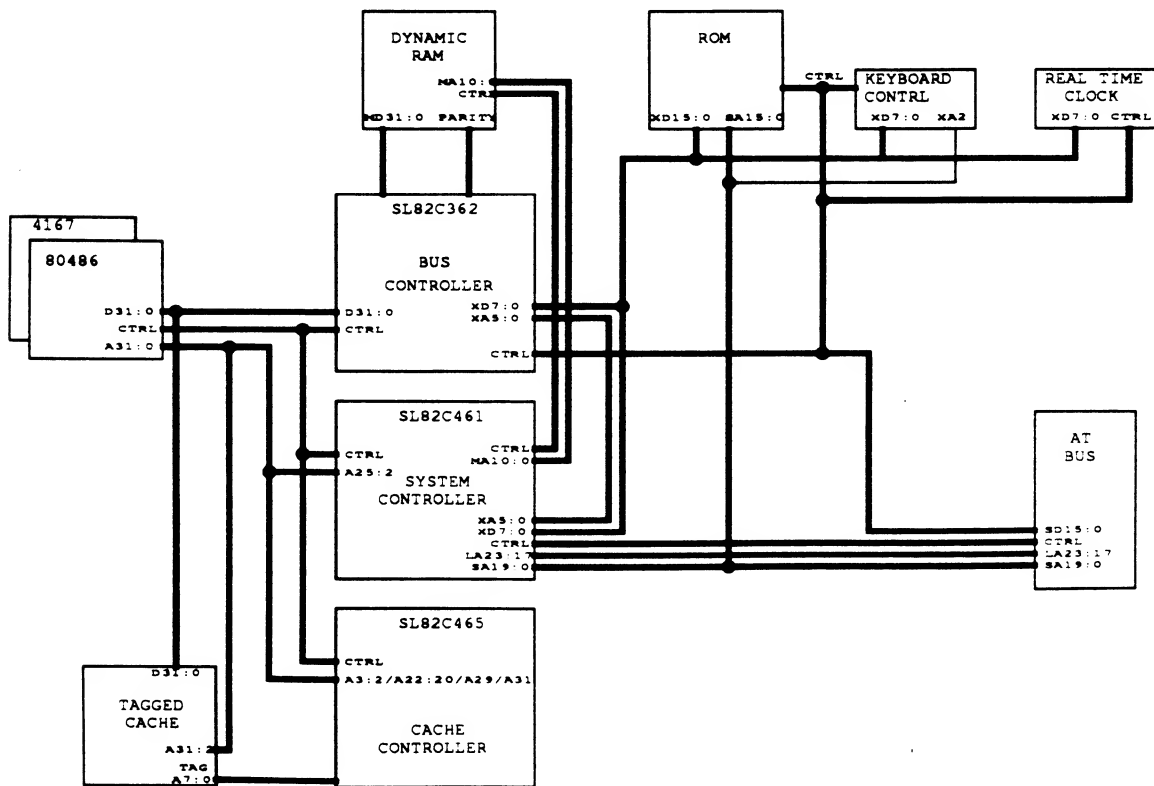
**Manufacturer:** Symphony Labs  
**Processor Supported:** 80386SX/DX  
**System Bus:** AT  
**Part:** SL82C465, 486 Cache Controller  
**Availability:** ?

**Cache:** Yes  
**Clock Speed:** 25, 33, 40 & 50 MHz  
**Main Memory Support:** No

**Second Source:**

**Functions Contained:**

Supports 32KB to 1MB cache size (1 to 4 double words)  
2-1-1-1 Burst mode cache fill  
Tag comparison and posted write control  
Non-cacheable region support  
Support for both 1X and 2X CPU clock



Symphony Labs SL82C460 486 Chipset

**Manufacturer:** Symphony Labs

**Processor Supported:** 80486DX/SX, 89386DX

**System Bus:** AT

**Part:** SL82C471, Cache/DRAM Controller (part of SL82C470 EISA Chip Set)

**Availability:**

**Second Source:**

**Functions Contained:**

Supports write-back cache

Page-mode DRAM

Supports 256K, 1M, 2M & 16MB DRAMS

Supports 64KB - 1MB cache

Snoop filtering & local bus support

Non-cacheable region support

**Cache:** Yes

**Clock Speed:** 25, 33, 40 & 50 MHz

**Main Memory Support:** Yes

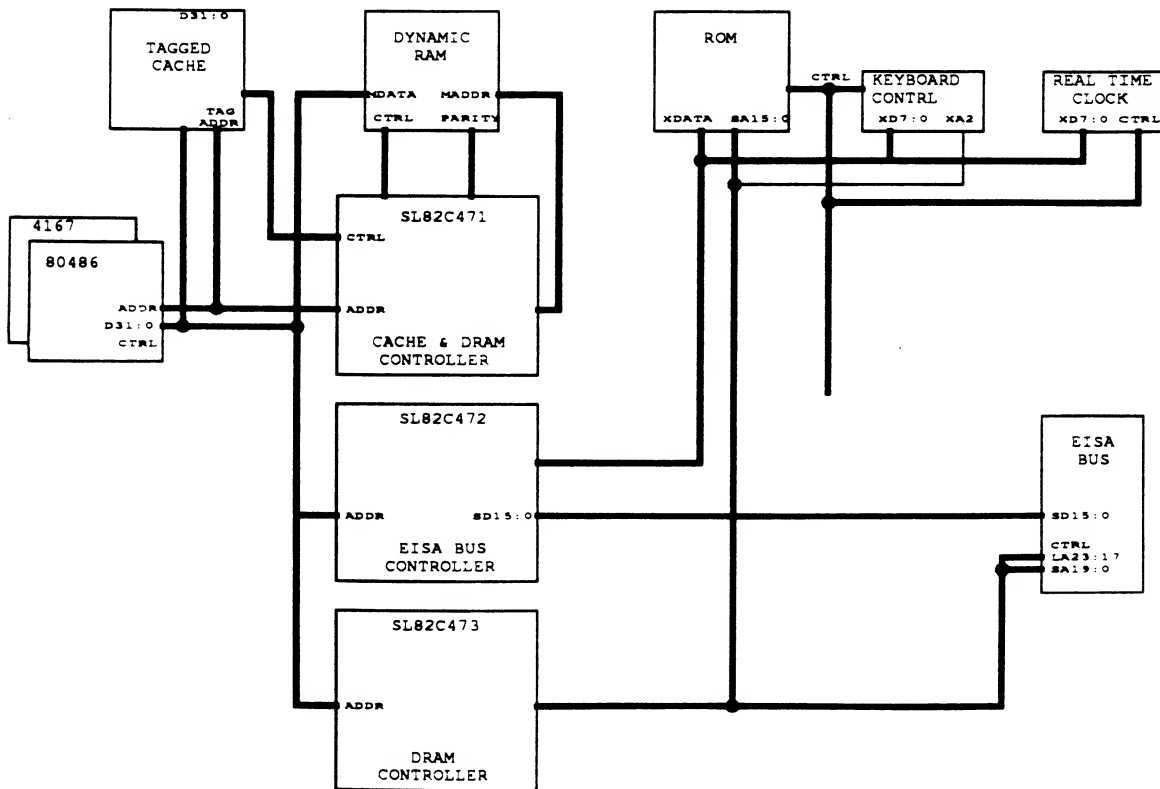
Supports shadowed BIOS

Zero-wait state DMA burst

2-1-1-1 Burst mode cache fill

Tag comparison and posted write control

Support for both 1X and 2X CPU clock



Symphony Labs SL82C470 486 Chipset

**Manufacturer:** Symphony Labs

**Processor Supported:** 80486DX/SX, 89386DX

**System Bus:** AT

**Part:** SL82C472, EISA Bus Controller (part of SL82C470 EISA Chip Set)

**Availability:** ?

**Second Source:**

**Functions Contained:**

(2) 8259 compatible interrupt controllers

(4) 8254 compatible timers

Provides parity generation/check logic

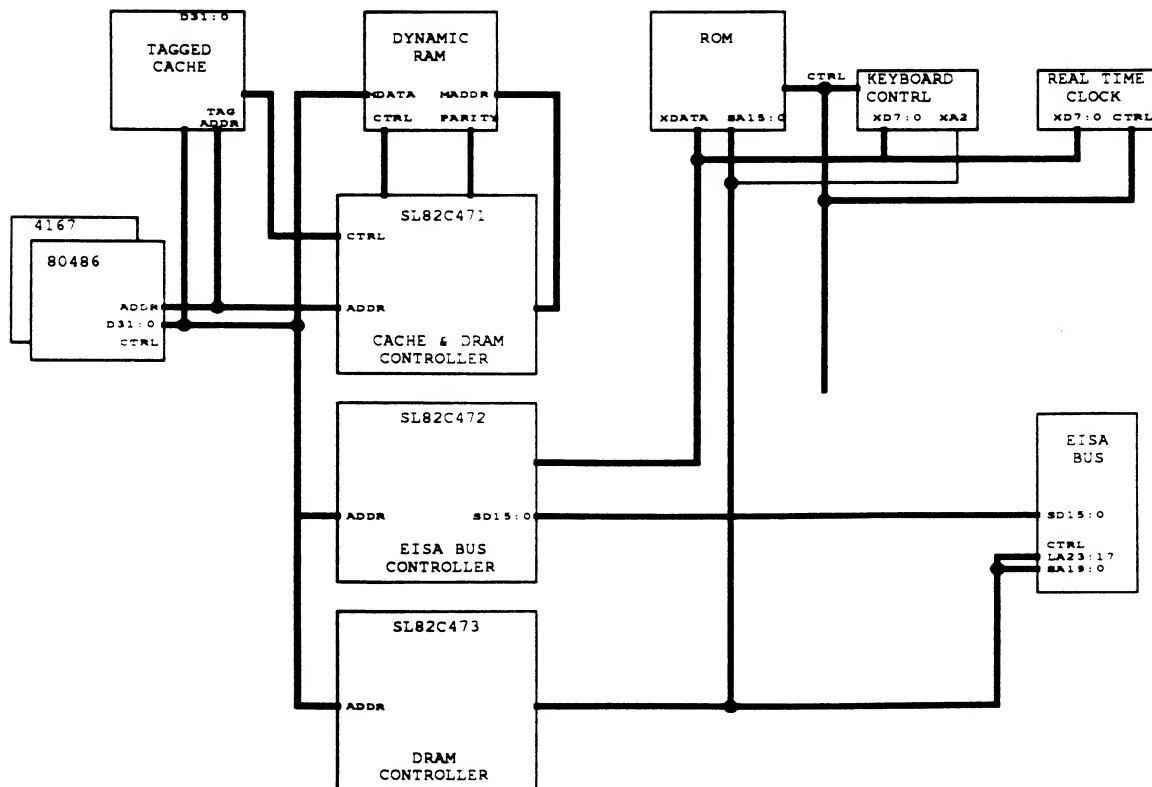
Provides NMI & time-out logic

Provides translation & alignment between CPU, EISA./ISA & DMA busses

**Cache:** No

**Clock Speed:** 25, 33, 40 & 50 MHz

**Main Memory Support:** No



Symphony Labs SL82C470 486 Chipset

**Manufacturer:** Symphony Labs

**Processor Supported:** 80486DX/SX, 89386DX

**System Bus:** EISA

**Part:** SL82C473, EISA DMA Controller (part of SL82C470 EISA Chip Set)

**Availability:** ?

**Second Source:**

**Functions Contained:**

Provides seven EISA DMA channels, system arbiter & co-processor interface logic

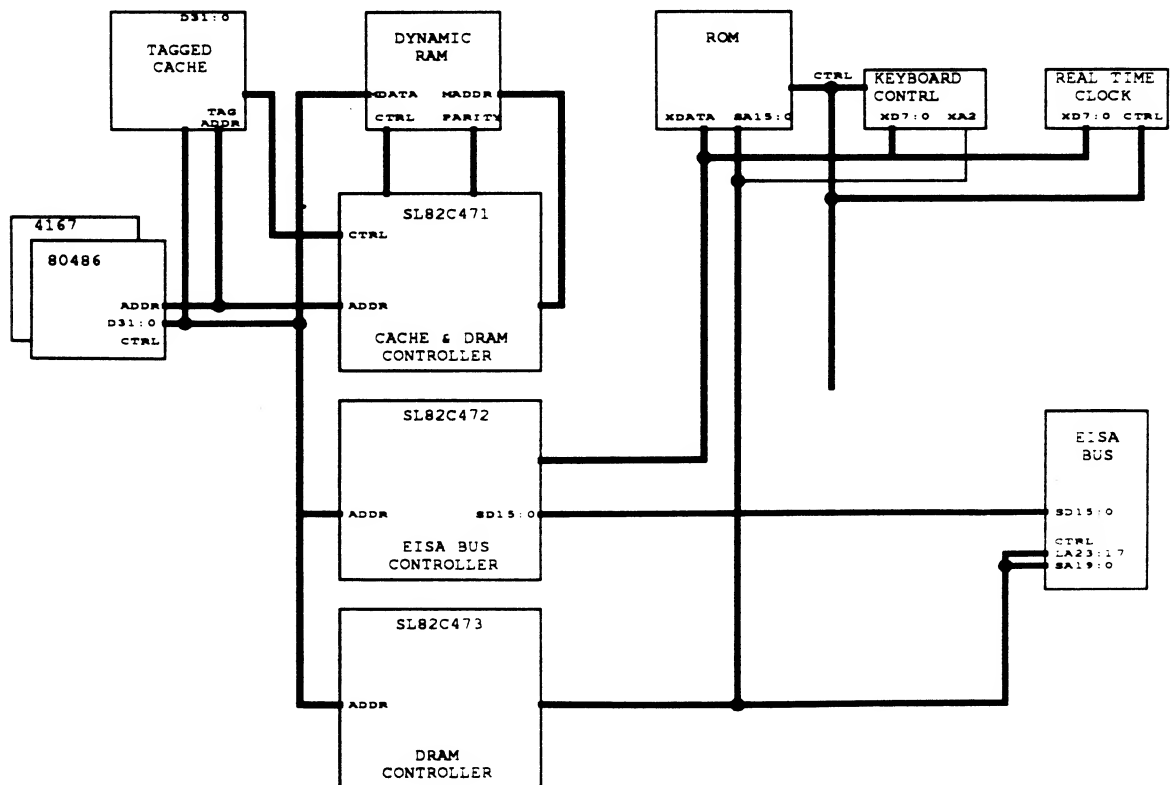
Provides address latches & buffers

Supports type A, B, C mode operations

**Cache:** No

**Clock Speed:** 25, 33, 40 & 50 MHz

**Main Memory Support:** No



Symphony Labs SL82C470 486 Chipset



**Manufacturer:** Texas Instruments  
**Processor Supported:** 80386SX, i486  
**System Bus:** AT  
**Part:** TACT82411, Single Chip AT  
**Availability:** 1990

**Cache:** No  
**Clock Speed:** 20 MHz (0 wait)  
**Main Memory Support:** Yes

**Second Source:** compatible with NEAT CHIPSet

**Functions Contained:**

(two) 8237 compatible DMA Controllers

(three) 8254 compatible timer/counter

(one) 74LS612 Page

Programmable DMA Clock

Shadow RAM support

Programmable memory configuration

Independent, asynchronous clock sources for CPU & ISA busses

(two) 8259A compatible Interrupt Controllers

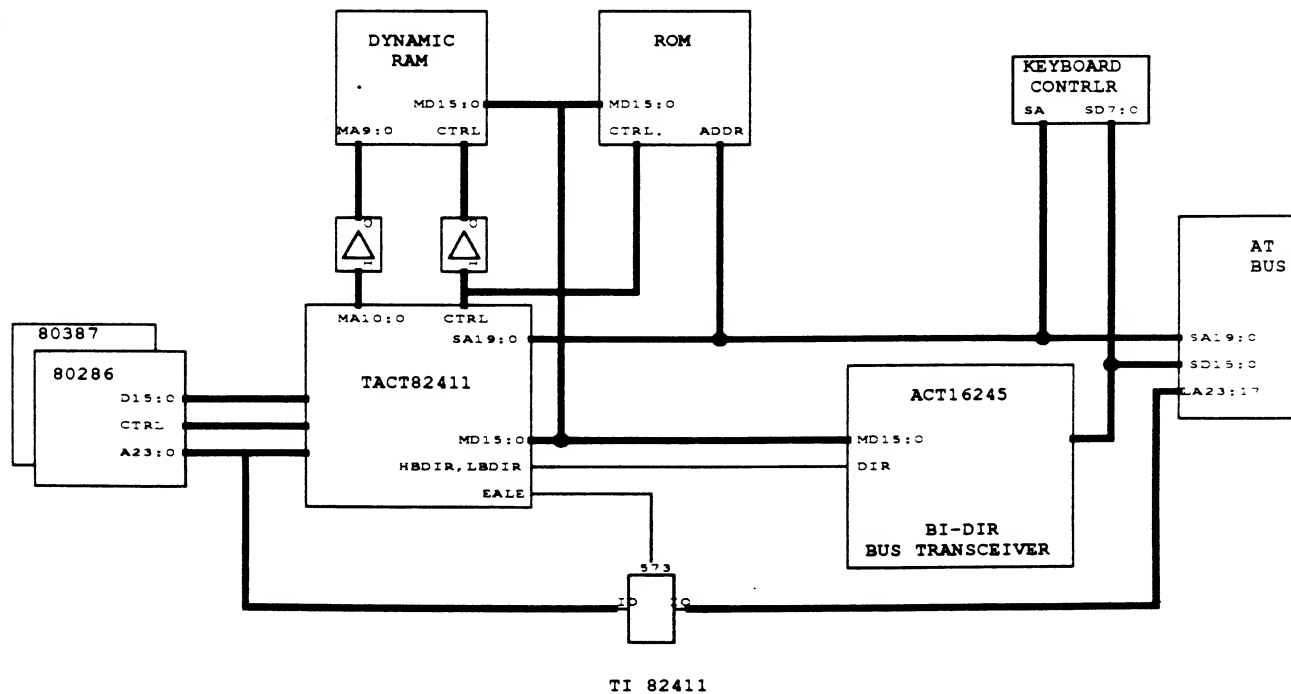
(one) Real Time Clock (RTC)

128 bytes of battery backup CMOS RAM/RTC Registers

DRAM support for 64K to 1M-bit DRAM

Programmable wait states

A20 gate & CPURST support



**Manufacturer:** Texas Instruments

**Processor Supported:** 80386SX, i486

**System Bus:** AT

**Part:** TACT83441, Data Path Unit (part of TACT83000 Chipset)

**Availability:** 1990

**Second Source:** ?

**Functions Contained:**

Cascadable (up to 8 MCUs)

16-bit CPU / I/O channel / Extended Local data bus support

8-bit peripheral bus (XD) support

One level cache "posted" write buffer

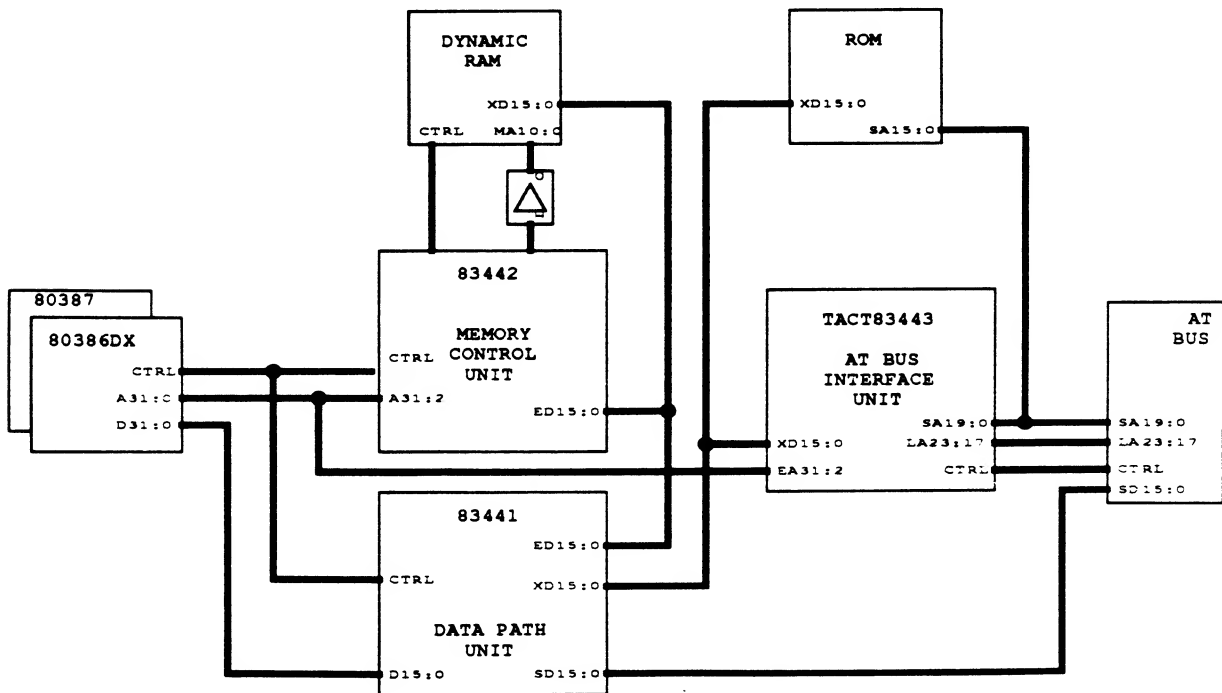
Parity check/generation for Extended Local bus

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**Cache:** No

**Clock Speed:** 33 MHz

**Main Memory Support:** Yes



TI 386DX Non-Cache

**Manufacturer:** Texas Instruments  
**Processor Supported:** 80386SX, i486

**System Bus:** AT

**Part:** TACT83442, Memory Control Unit (part of TACT83000 Chipset)

**Availability:** 1990

**Second Source:** ?

**Functions Contained:**

Addresses up to 32M Bytes of main memory

Page mapping SRAM

Programmable DRAM parameters

ROM chip select logic

**Cache:** No

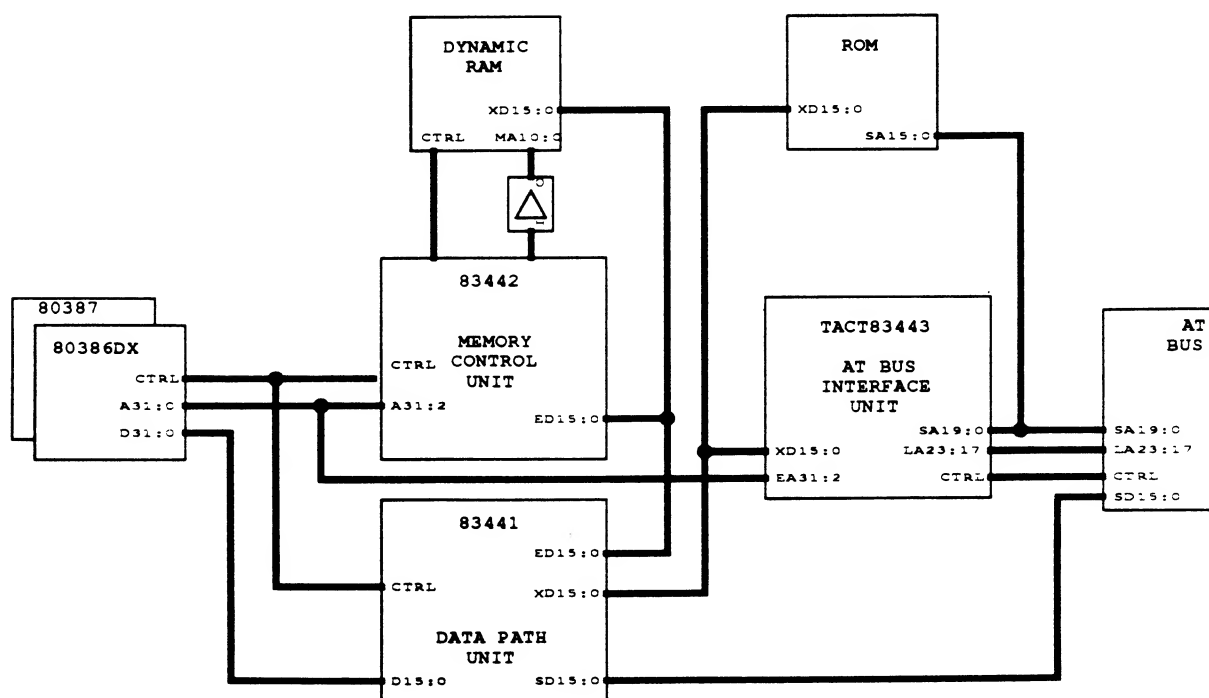
**Clock Speed:** 33 MHz

**Main Memory Support:** Yes

Cascadable (up to 8 MCUs)

Supports 256K, 1M, 4M-bit DRAMS

Normal, page and 2-way/4-way interleave memory access



TI 386DX Non-Cache

**Cache: No**

**Clock Speed: 33 MHz**

**Main Memory Support: No**

**Part:** TACT83443, AT Bus Interface Unit (part of TACT83000 Chipset)

**Availability:** 1990

**Second Source: ?**

### Functions Contained:

**(two) 8237 compatible DMA Controllers**

**(two) 8259A compatible Interrupt Controllers**

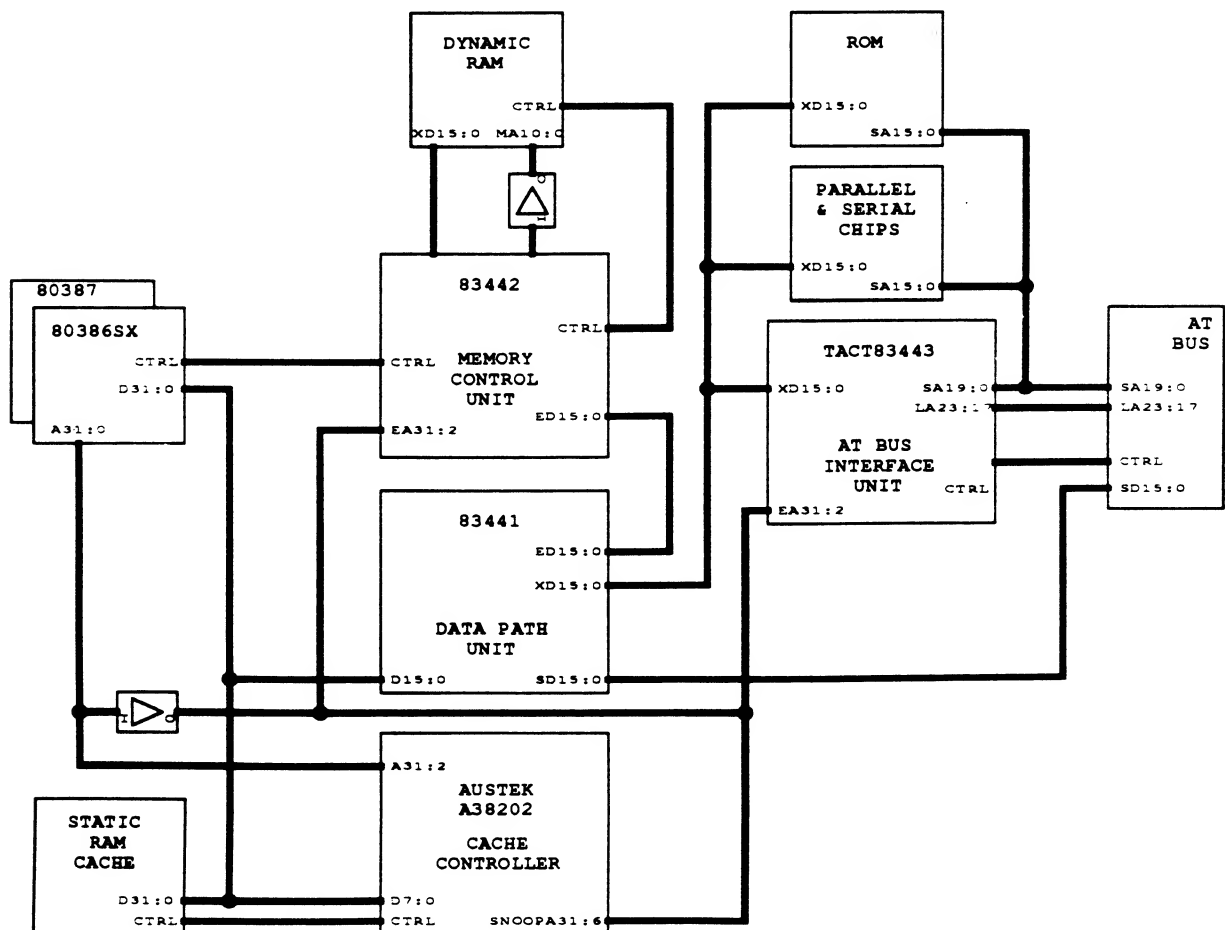
(three) 8254 compatible timer/counter

(one) 146818 compatible Real Time Clock (RTC)

**128 bytes of battery backup CMOS RAM/RTC Registers**

### Port B & NMI

## Program Timing Control



**Manufacturer:** United Micro Electronics (UMC)

**Processor Supported:** 80286

**System Bus:** AT

**Part:** UM82C206, Integrated Peripheral Controller (part of 82C230 AT Chip Set)

**Availability:**

**Second Source:**

**Functions Contained:**

(two) 8237 compatible DMA Controllers

(one) 8254 compatible timer/counter

(one) 74LS612 memory mapper

**Cache:** No

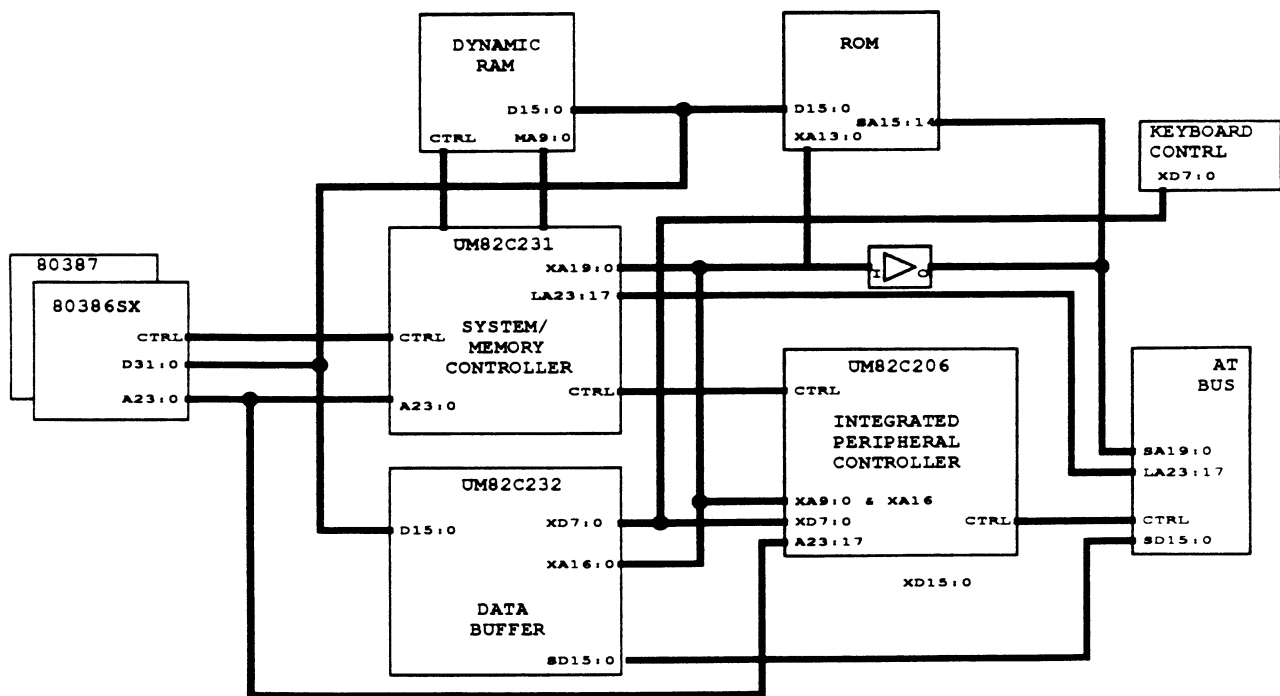
**Clock Speed:** 10 & 12 MHz

**Main Memory Support:** No

(two) 8259A compatible Interrupt Controllers

(one) MC146818 compact Real Time Clock

114 bytes CMOS RAM



UMC UM82C230 286 PC/AT Chipset

**Manufacturer:** United Micro Electronics (UMC)

**Processor Supported:** 80286

**System Bus:** AT

**Part:** UM82C231, System/Memory Controller (part of 82C230 AT Chip Set)

**Availability:**

**Second Source:**

**Functions Contained:**

EPROM chip select support

CPU interface/bus control

Refresh & DMA logic

8087 interface

**Cache:** No

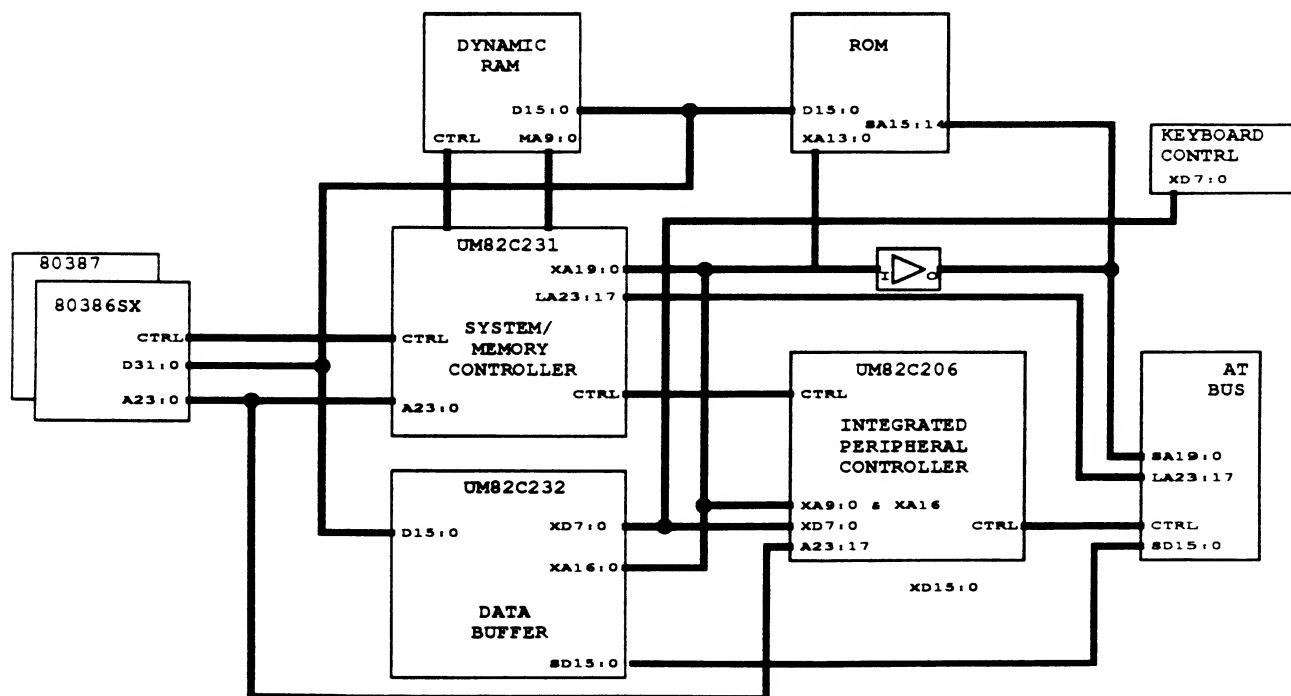
**Clock Speed:** 12MHz (0 wait)

**Main Memory Support:** Yes

1 to 4MB on board memory (64KB-256KB, 1MB DRAMS)

Clock generation

Reset & shut down logic



UMC UM82C230 286 PC/AT Chipset

**Manufacturer:** United Micro Electronics (UMC)

**Processor Supported:** 80286

**System Bus:** AT

**Part:** UM82C232, Data Buffer Controller (part of 82C230 AT Chip Set)

**Availability:**

**Second Source:**

**Functions Contained:**

Provides 16-bit or 8-bit buffering between CPU bus & AT bus

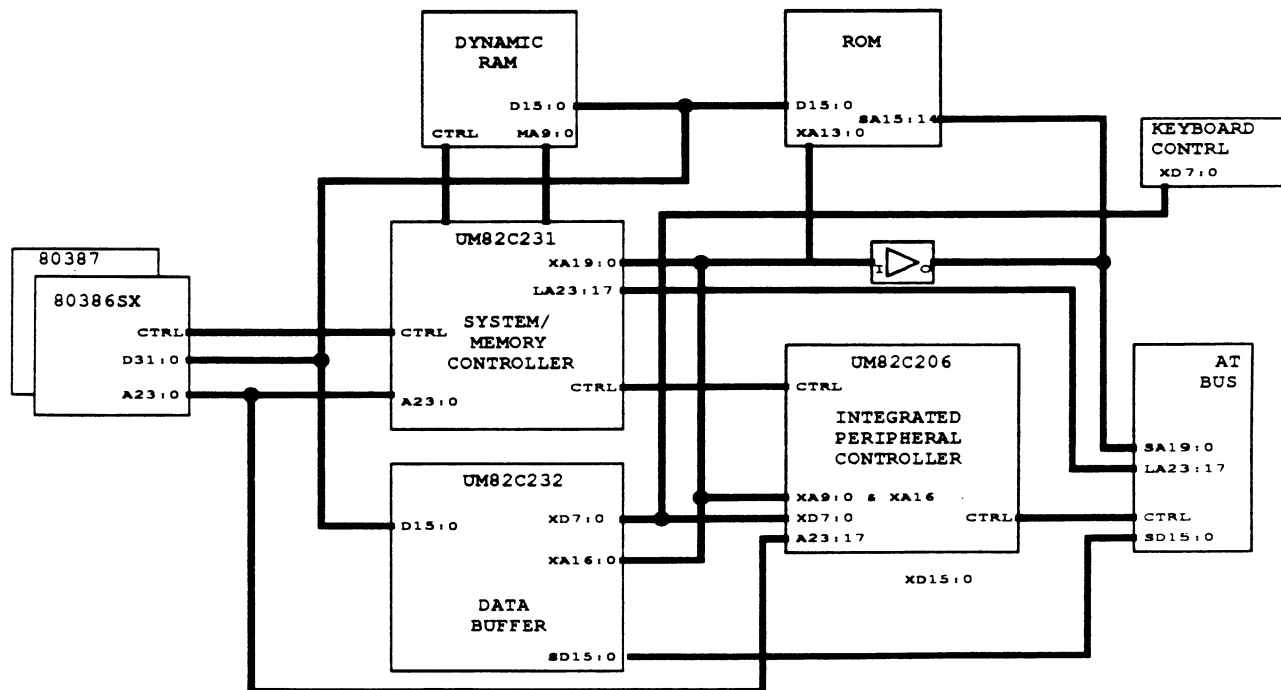
8-bit I/O port data bus buffering

Parity generation/detection

**Cache:** No

**Clock Speed:** 10 & 12 MHz

**Main Memory Support:** No



UMC UM82C230 286 PC/AT Chipset

**Manufacturer:** United Micro Electronics (UMC)

**Processor Supported:** 80386

**System Bus:** AT

**Part:** UM82C481, Integrated Memory Controller (part of 82C230 AT Chip Set)

**Availability:**

**Second Source:**

**Functions Contained:**

Cache controller (direct mapped, programmable cache line size)

Supports 32/64/128/256/512, 1MB cache size

Interleaved cache RAM support

Supports fast A20 gate

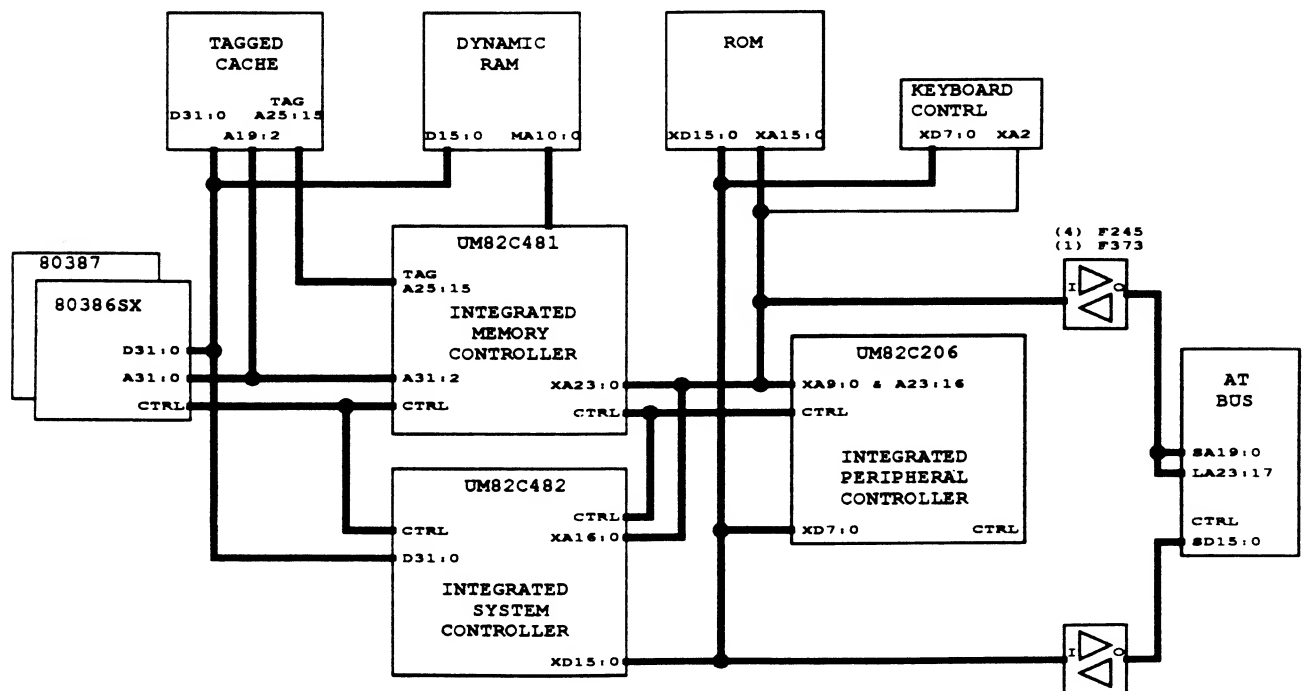
**Cache:** Yes

**Clock Speed:** 25, 33, 40 & 50 MHz

**Main Memory Support:** Yes

DRAM controller (up to 64MB) - page mode  
3 independent non-cacheable region

80387 / WT3167 / WT4167 interface logic



UMC UM82C230 286 PC/AT Chipset



**Manufacturer:** United Micro Electronics (UMC)

**Processor Supported:** 80386

**System Bus:** AT

**Part:** UM82C482, Integrated System Controller

**Availability:**

**Second Source:**

**Functions Contained:**

AT Bus control logic

CPU reset logic

Parity generation/detection logic

Timer

**Cache:** No

**Clock Speed:** 25, 33, 40 & 50 MHz

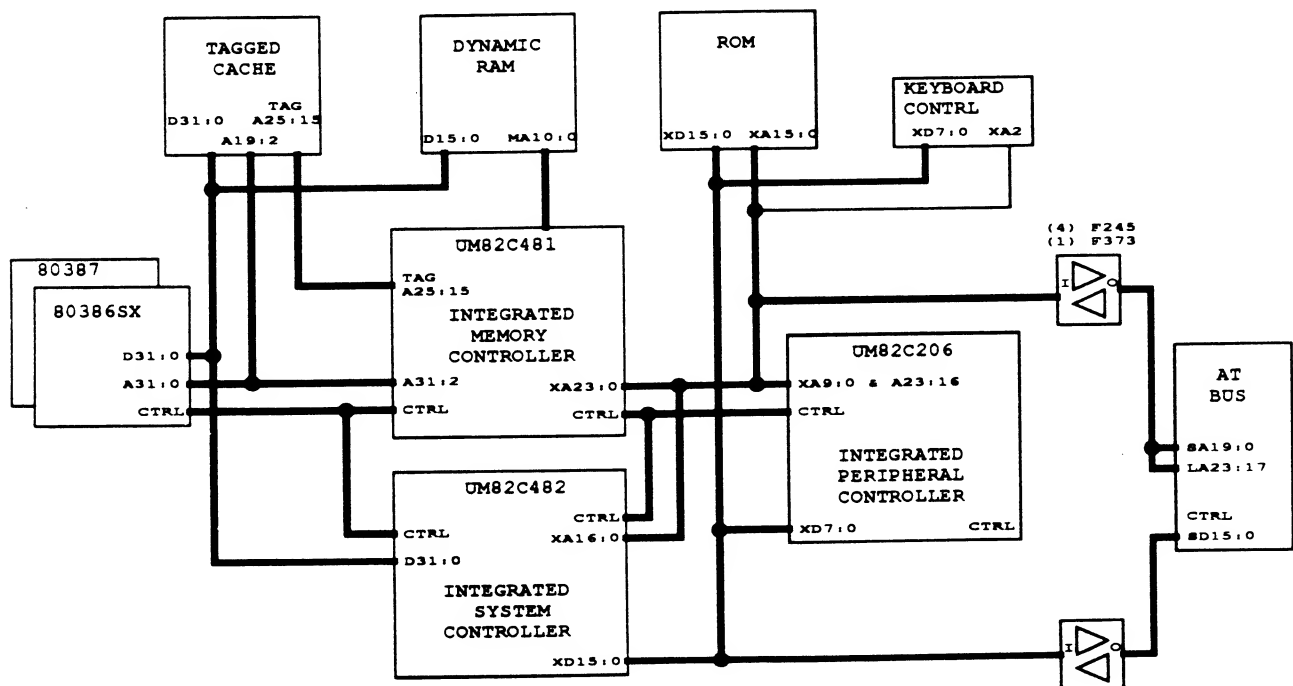
**Main Memory Support:** Yes

Data Bus conversion logic

Clock generation for CPU, keyboard, and DMA/Refresh logic

Peripheral interface logic

256KB/512KB/1MB EPROM support



UMC UM82C230 286 PC/AT Chipset



**Manufacturer:** Vadem  
**Processor Supported:** 8088/8086  
**System Bus:** XT  
**Part:** VG-230, Sub-notebook engine  
**Availability:** 1991 Q4  
**Second Source:**

**Functions Contained:**

16-bit NEC V30HL CPU  
Power management (+5V and +3V available)  
(one) 8237A DMA Controller  
Real Time Clock (RTC)  
Parallel port  
System Management Unit  
ISA bus interface Unit  
Memory manager (DRAM, PSRAM, SRAM)  
Memory controller: (eight) 8-bit RAM banks or (six) 16-bit RAM banks

**Cache:** No  
**Clock Speed:** 16 MHz  
**Main Memory Support:** Yes

Keyboard scanner  
Serial port (16450 UART compatible)  
(one) 8259A Interrupt controller  
(one) 8254 clock/timer  
Timer  
PCMCIA A & B (PC card slots)  
VGA LCD controller (optional)

Schematic Not Available At Press Time

## Personal Computer Design

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**Manufacturer:** VLSI

**Processor Supported:** 8086, or V30

**System Bus:** XT

**Part:** VL82C031-FC, Super XT-compatible System Controller

**Availability:** ?

**Second Source:**

**Functions Contained:**

Supports 8M bytes of expanded memory (EMS 4.0)

Provides 4 channels of 8 MHz DMA (also burst mode)

Arbitrates system bus among the CPU, DMA math coprocessor and DRAM refresh cycles

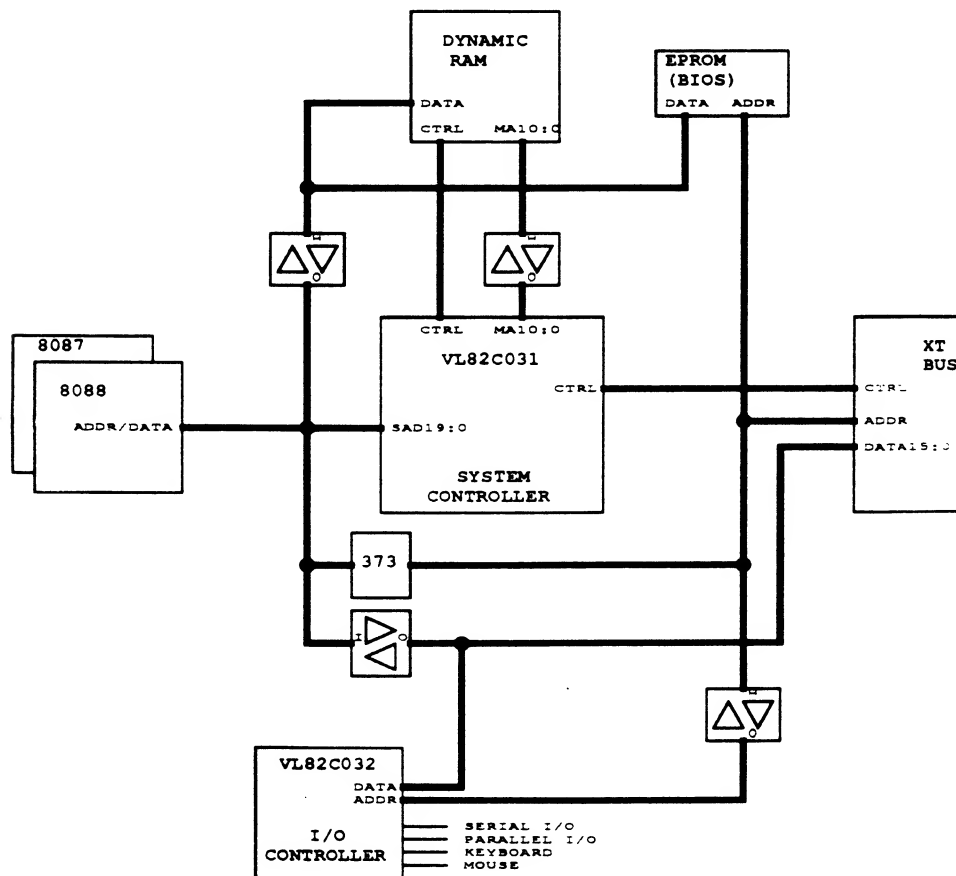
**Cache:** No

**Clock Speed:** 8 or 10 MHz

**Main Memory Support:** Yes

Supports 256K or 1M bit DRAMs

Power down mode support logic



VLSI : XT Chipset

**Manufacturer:** VLSI

**Processor Supported:** 8086, or V30

**System Bus:** XT

**Part:** VL82C032-FC, Super XT-compatible I/O Controller

**Availability:** ?

**Second Source:**

**Functions Contained:**

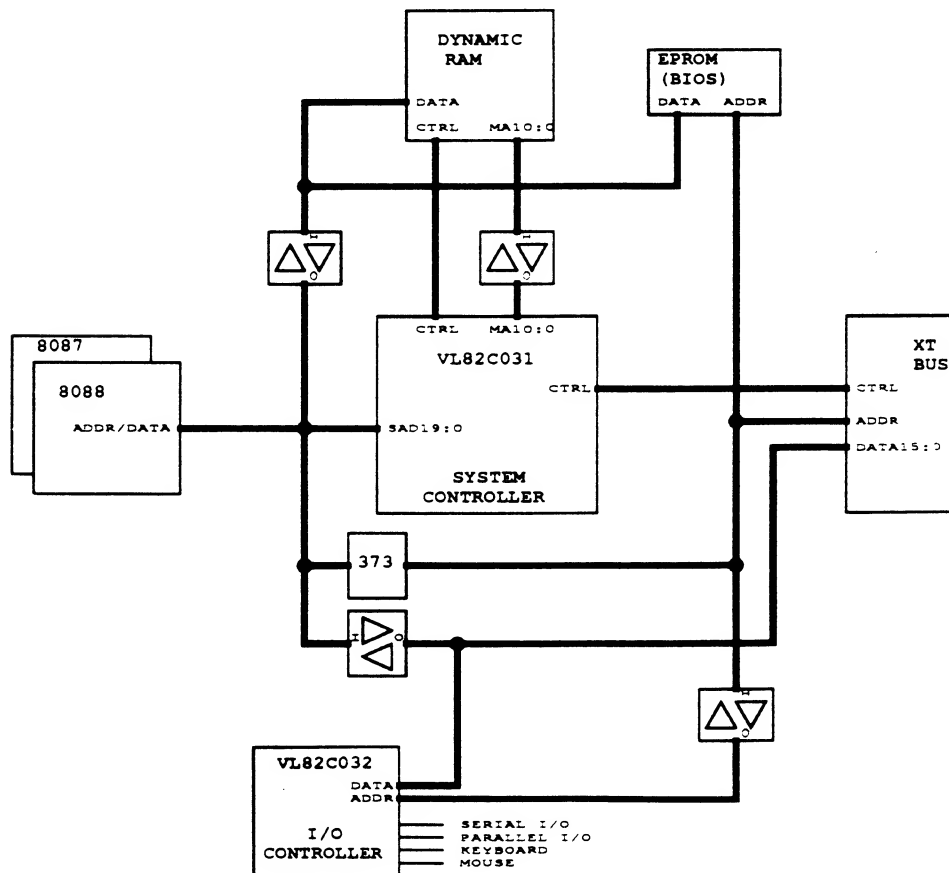
(one) 8253 compatible Timer/Counter

(two) 8250 compatible Serial Communications Controller

(one) 8259A compatible Interrupt Controller

(one) 58167 compatible Real Time Clock (RTC)

Bidirectional Parallel Port Controller



VLSI : XT Chipset

## **Personal Computer Design**

---

**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL86C050, I/O Processor

**Availability:** ?

**Second Source:** ?

**Functions Contained:**

On-chip 32-bit RISC microprocessor (VL86C010)

On-chip RAM (128 32-bit words)

ISA address decoding with programmable wait states

Peripheral controller

Interrupt logic

Watch Dog timer

DRAM controller (up to 16MB, four banks, page mode, 2/4 way interleave)

---

**Cache:** No

**Clock Speed:** 10 MHz

**Main Memory Support:** Yes

On-chip ROM (512 32-bit words)

ISA bus interface (with drivers)

DMA controller

Abort logic

(two) Interval timers

**Schematic Not Available At Press Time**

**Manufacturer:** VLSI

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C37A-08PC, CMOS Direct Memory Access Controller

**Availability:** ?

**Second Source:** Compatible with standard 8237 DMA controllers

**Functions Contained:**

Four DMA channels

Individual enable/disable control of DMA requests

Directly expandable

Independent auto-initialize feature

---

**Schematic Not Available At Press Time**

## Personal Computer Design

**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C100, PC/AT Compatible Peripheral Controller (part of VL82CPCAT-16 Chip set)

**Availability:** 1987

**Second Source:** ?

**Functions Contained:**

(two) 82C37A compatible DMA Controllers

(one) 82C54 compatible timer/counter

(one) 74ALS373 Octal Tri-State Latch

**Cache:** No

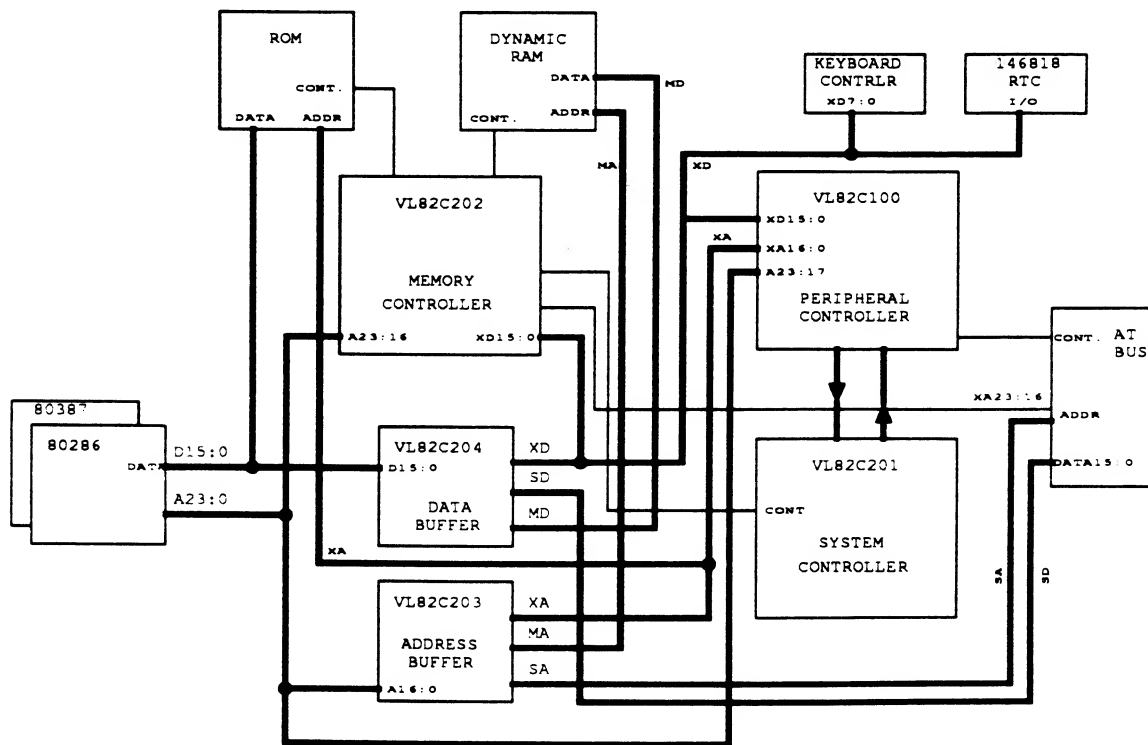
**Clock Speed:** 12 or 16 MHz

**Main Memory Support:** No

(two) 82C59A compatible Interrupt Controllers

(one) 74LS612 compatible Memory Mapper

(one) 74ALS138 3-to-8 decoder



VLSI VL82CPCAT-16

BA



**Processor Supported:** 80286

**Clock Speed:** 12 MHz

**System Bus:** AT

**Main Memory Support:** No

**Part:** VL82C101B, PC/AT Compatible System Controller

**Availability:** 1987

**Second Source:** ?

**Functions Contained:**

(one) 82C284 compatible Clock Controller

(one) 82C288 compatible Bus Controller

(one) 82C84A compatible Clock Generator and driver

(two) PAL16L8 devices (memory decode)

Wait state logic

---

**Schematic Not Available At Press Time**

## **Personal Computer Design**

---

**Manufacturer:** VLSI Technology

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C102, PC/AT Compatible Memory Controller

**Availability:** 1987

**Second Source:**

**Functions Contained:**

Addresses up to 4MB

ROM chip select logic

**Cache:** No

**Clock Speed:** 12 MHz

**Main Memory Support:** Yes

Upper addresses for I/O slots

Speaker driver

---

Schematic Not Available At Press Time

**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C103, PC/AT Compatible Address Buffer

**Availability:** 1987

**Second Source:** ?

**Functions Contained:**

Provides 16-bit address buffer from Local bus (LA) to System (SA) and Peripheral (XA) busses

Refresh (256K-bit & 1M-bit DRAMS)

---

**Cache:** No

**Clock Speed:** 12 MHz

**Main Memory Support:** Yes

Schematic Not Available At Press Time

## **Personal Computer Design**

---

**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C104, PC/AT Compatible Data Buffer

**Availability:** 1987

**Second Source:** ?

**Functions Contained:**

Provides 16-bit data CPU (D) bus, System (SD) bus and Peripheral (XD) bus buffer and Memory Data (MD) bus drivers

Parity generator/detector

---

**Cache:** No

**Clock Speed:** 12 MHz

**Main Memory Support:** Yes

Schematic Not Available At Press Time

**Manufacturer:** VLSI  
**Processor Supported:** 80286  
**System Bus:** AT  
**Part:** VL82C106-FC, PC/AT Combo I/O Chip  
**Availability:** ?

**Cache:** No  
**Clock Speed:** ? MHz  
**Main Memory Support:** No

**Second Source:**

**Functions Contained:**

(two) VL16C450 UARTs

(one) 80C42 compatible Keyboard/Mouse Controller

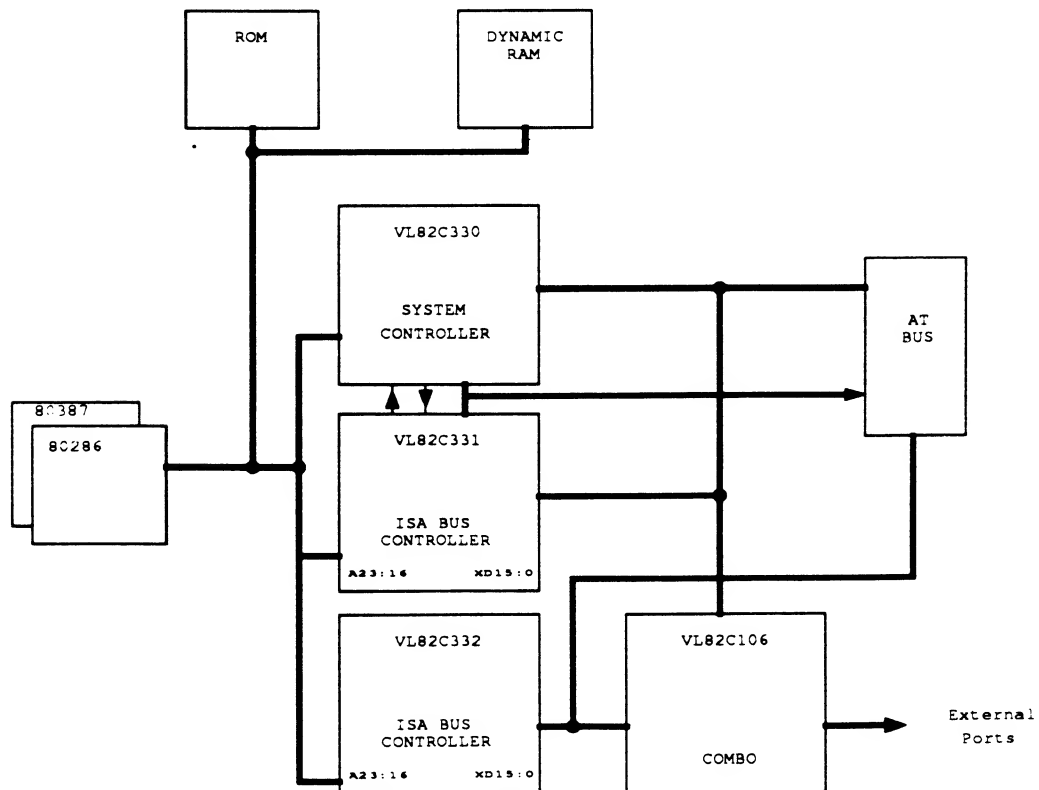
66 bytes of standby RAM

Programmable chip select registers

(one) bidirectional Parallel Printer Port

(one) 146818A compatible Real Time Clock

IDE bus control signals



VLSI VL82CPCPM-16/20

## **Personal Computer Design**

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**Manufacturer:** VLSI Technology, Inc  
**Processor Supported:** 80286, 80386SX  
386)  
**System Bus:** AT  
**Part:** VL82C107, SCAMP Combination Chip  
**Availability:** 1991  
**Second Source:** ?  
**Functions Contained:**  
Used in conjunction with SCAMP DT Controller  
146818A compatible Real Time Clock (RTC)  
Address latches/buffers  
PC Memory card interface  
14.3181 MHz clock

---

**Cache:** No  
**Clock Speed:** 10-20 MHz (25 w/ System P  
**Main Memory Support:** No

AT compatible Keyboard/mouse controller  
128 bytes of battery backed CMOS RAM  
DMA Acknowledge decoder  
8-bit or 16-bit memory card supportIntegrated

Schematic Not Available At Press Time

**Manufacturer:** VLSI Technology, Inc  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT  
**Part:** VL82C108, TOPCAT Combo I/O Chip  
**Availability:** 1990  
**Second Source:** ?

**Cache:** No  
**Clock Speed:** ?  
**Main Memory Support:** No

**Functions Contained:**

(one) VL16C450 compatible UART  
IDE bus control signals (external buffers required)  
Keyboard/Mouse controller (PC/AT or PS/2 compatible)

Bidirectional parallel printer port  
Selectable chip select decodes

---

Schematic Not Available At Press Time

## **Personal Computer Design**

---

**Manufacturer:** VLSI Technology, Inc  
**Processor Supported:** 80286, 80386  
Xtal)

**System Bus:** AT

**Part:** VL82C110, Floppy Disk Controller Combo Chip

**Availability:** 1991

**Second Source:** pin compatible with National PC87310

**Functions Contained:**

765A compatible floppy disk controller with digital

(two) VL16C450 UARTS (COM1 - COM4)

IDE bus control signals

**Cache:** No

**Clock Speed:** 24 MHz (System Bus -

**Main Memory Support:** No

Data clock separator

Bidirectional parallel printer port (LPT1 - LPT3)

Power Management Unit

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Schematic Not Available At Press Time



**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C201, PC/AT Compatible System Controller (part of VL82CPCAT-16 Chip set)

**Availability:** 1988

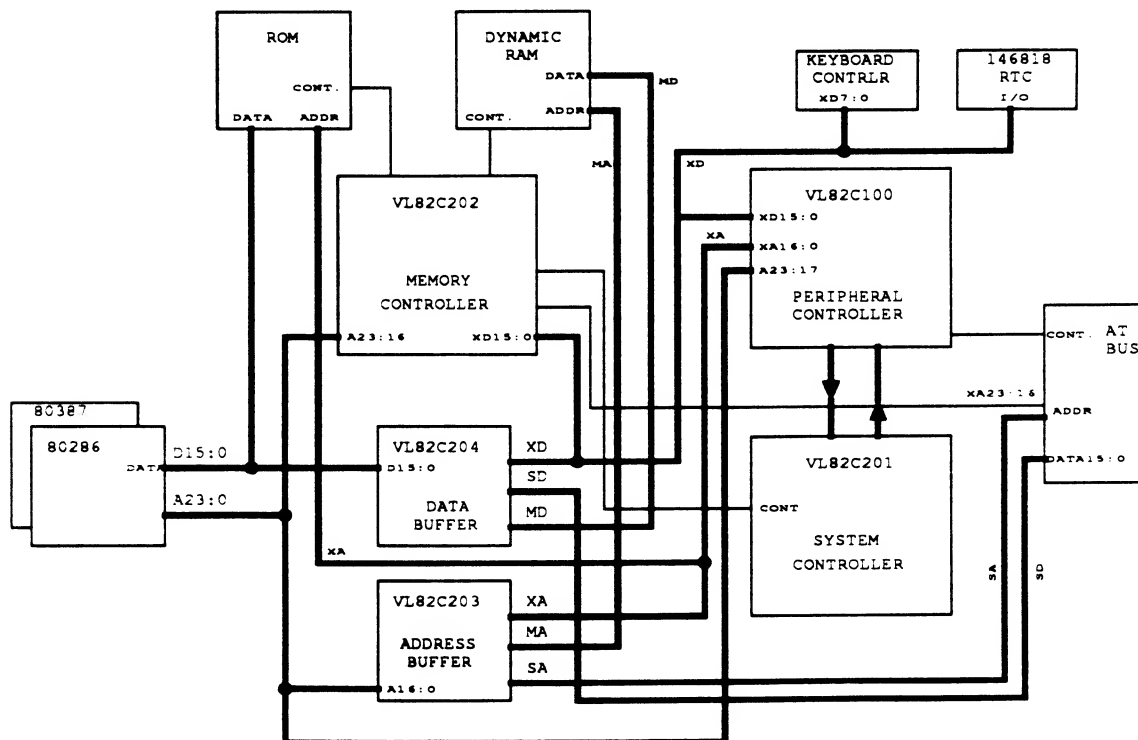
**Second Source:** ?

**Functions Contained:**

(one) 82C284 compatible Clock Controller

(one) 82C288 compatible Bus Controllers

(one) 82C84A compatible Clock Generator and driver (two) PAL16L8 devices (memory decode)



VL82CPCAT-16

SA

## Personal Computer Design

**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C202, PC/AT Compatible Address Buffer (part of VL82CPCAT-16 Chip set)

**Availability:** 1988

**Second Source:** ?

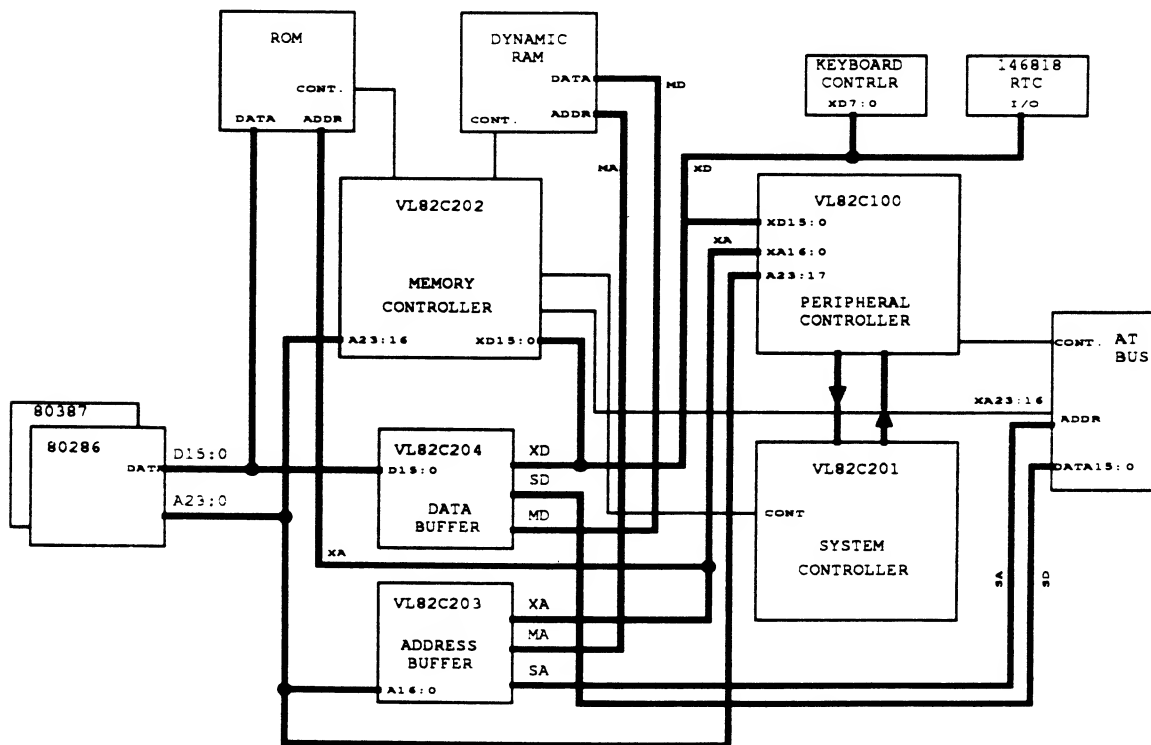
**Functions Contained:**

Provides 16-bit address buffer from Local bus (LA) to System (SA) and Peripheral (XA) busses  
Refresh (256K-bit & 1M-bit DRAMS)

**Cache:** No

**Clock Speed:** 16 MHz

**Main Memory Support:** Yes



VLSI VL82CPCAT-16

SA

**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80286

**System Bus:** AT

**Part:** VL82C204, PC/AT Compatible Data Buffer (part of VL82CPCAT-16 Chip set)

**Availability:** 1988

**Second Source:** ?

**Functions Contained:**

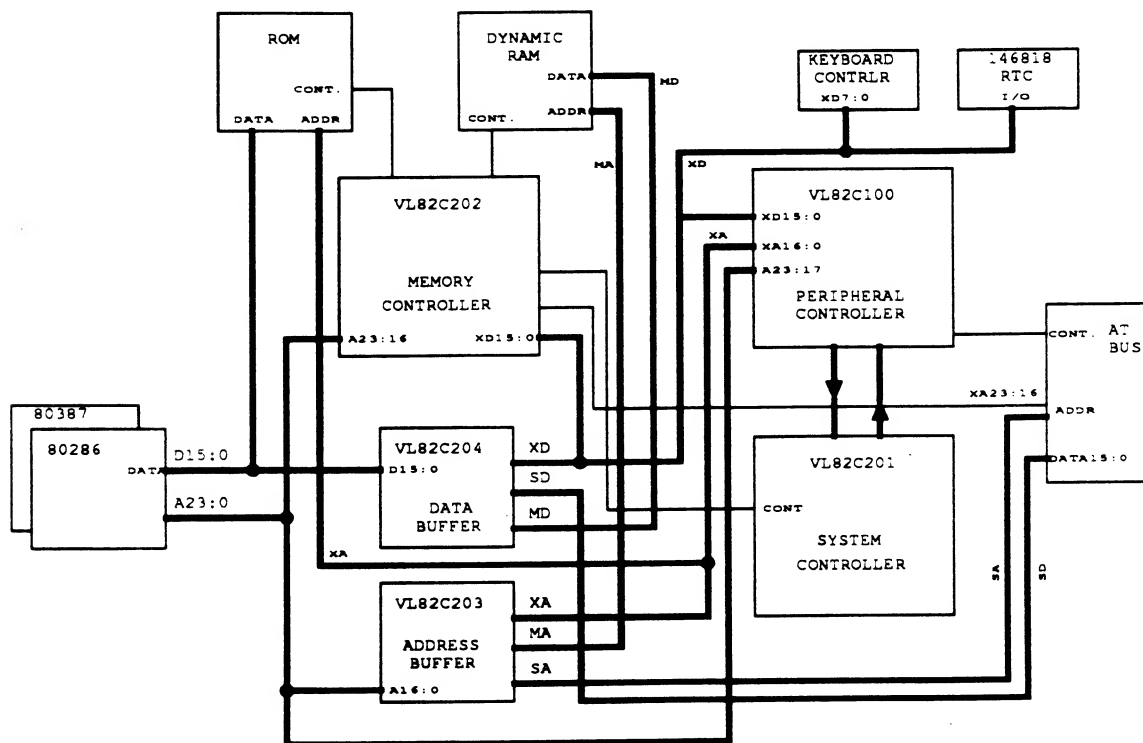
Provides 16-bit data CPU bus (D) buffer System (SD) bus and Peripheral (XD) bus

Parity generator/detector

**Cache:** No

**Clock Speed:** 16 MHz

**Main Memory Support:** Yes



VL82CPCAT-16

SA

## Personal Computer Design

**Manufacturer:** VLSI

**Processor Supported:** 80386SX

**System Bus:** AT

**Part:** VL82C205A -16QC -20QC, Page-Mode/Interleave Controller

**Availability:** ?

**Second Source:** Downward compatibility with VL82C205

**Functions Contained:**

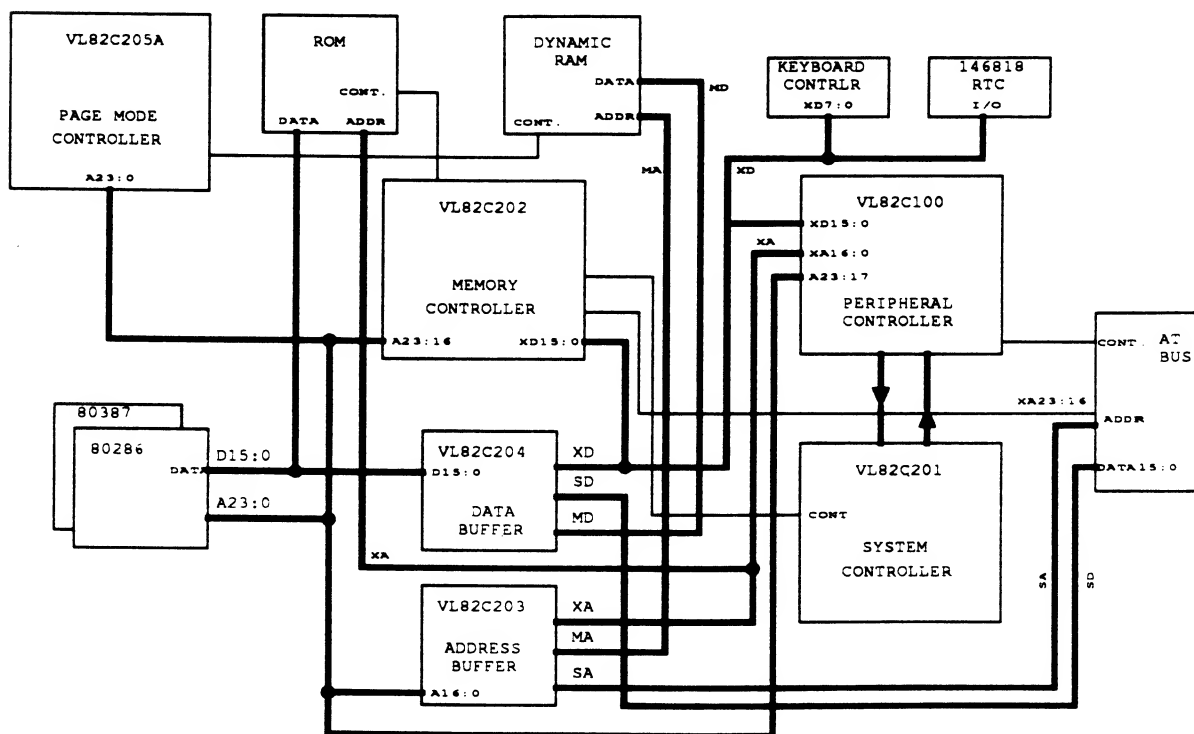
Supports two bank interleaved page-mode DRAM accesses

Average .6 wait state for 100ns DRAM

**Cache:** No

**Clock Speed:** 16 & 20 MHz

**Main Memory Support:** Yes



VLSI VL82CPCPM-16/20

SA

**Manufacturer:** VLSI Technology, Inc  
**Processor Supported:** 80386DX  
**System Bus:** AT  
**Part:** VL82C312, SCAMP Power Management Unit  
**Availability:** 1991

**Cache:** Yes  
**Clock Speed:** 20, 25 & 33 MHz  
**Main Memory Support:** No

**Second Source:**

**Functions Contained:**

Designed for laptop /notebooks

Provides system activity monitoring, peripheral control, power supply control, mode timers & general purpose I/O Independent programmable timers to power saving modes and LCD/backlight control

Provides five modes of operation (On, Doze, Sleep, Suspend, Off)

10 individual power control outputs (3 for LCD, 7 for general purpose)

Multiple power-on sources (pushbutton, RTC alarm, modem)

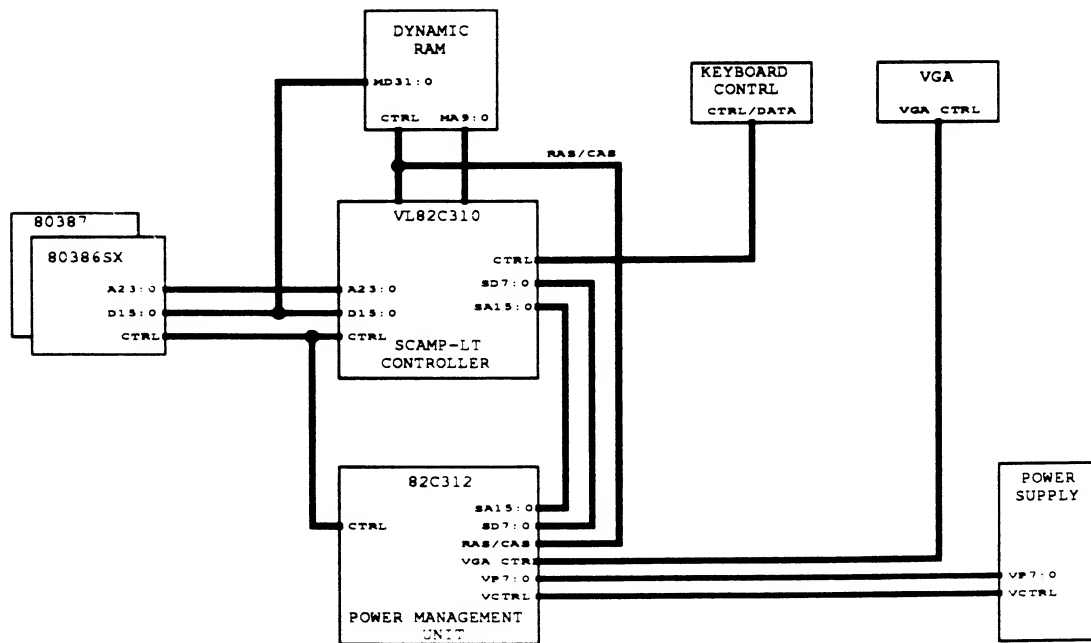
2 low level battery warning monitors

10 general purpose I/O ports

Programmable NMI generation

Provides chip selects for IDE, Floppy controller and VL16C452

Provides multiplexed address/data bus for VGA controller & VL16C452



VLSI 82C312 SCAMP Power Management Unit

## Personal Computer Design

---

**Manufacturer:** VLSI Technology, Inc  
**Processor Supported:** 8088, 80286, 80386, 80486  
**System Bus:** AT  
**Part:** VL82C322, Power Management Unit

**Cache:** Yes  
**Clock Speed:** ? MHz  
**Main Memory Support:** No

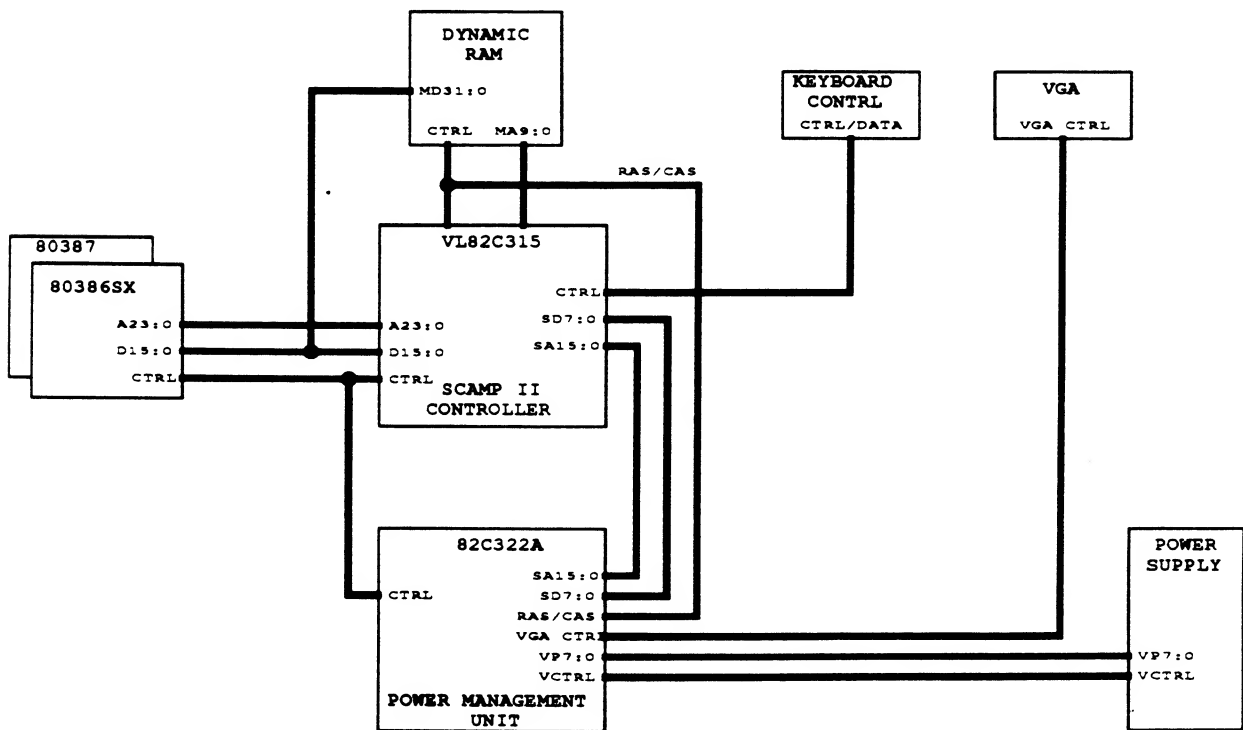
**Availability:** ?

**Second Source:** ?

**Functions Contained:**

Detects inactivity & removes power where necessary  
Provides independent timers for LCD backlight and display  
Controls power to eight external devices independently

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VLSI 82C322A SCAMP Power Management Unit

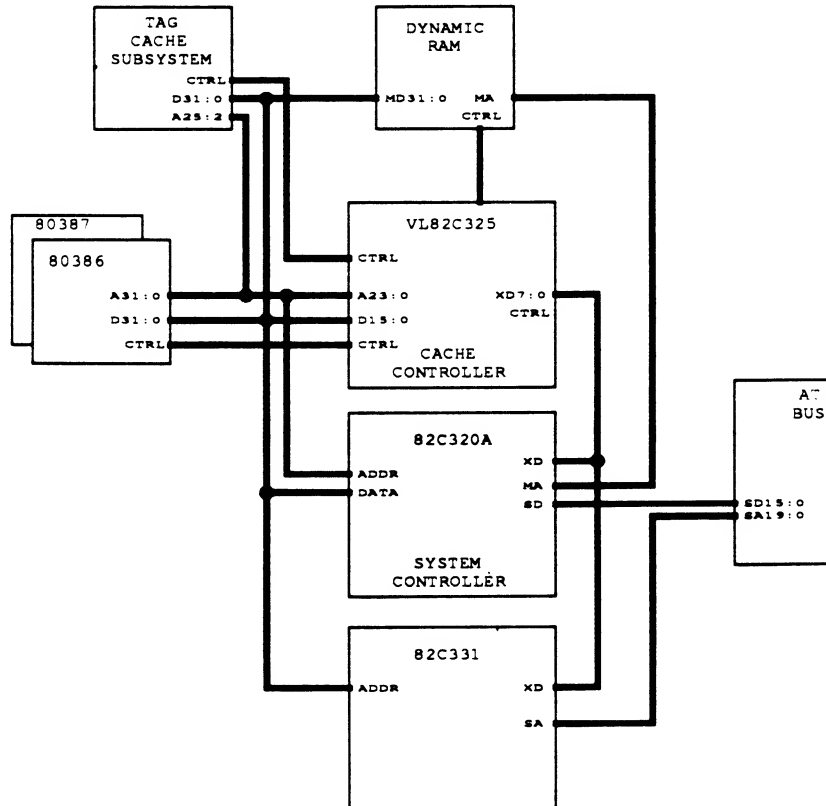
**Manufacturer:** VLSI Technology, Inc  
**Processor Supported:** 80286, 80386SX  
**System Bus:** AT  
**Part:** VL82C325, TOPCAT/SCAMP SX Cache Controller  
**Availability:** 1991

**Cache:** Yes  
**Clock Speed:** 20 & 25 MHz  
**Main Memory Support:** No

**Second Source:**

**Functions Contained:**

Supports 2-way set associative organization (16KB or 32KB)	Write-thru memory update strategy
Supports memory configurations up to 16MB	Write protect region support
Fast look-aside architecture (cache & main accessed in parallel)	Operates in Pipelined or Non-pipelined mode
Programmable cache architecture (2 byte line size, 4 or 8 line block size)	Works in parallel with VL82C320A or VL82C310/VLC311
Zero wait state read hit access	
Least Recently Used (LRU) replacement algorithm	
Non-cacheable region support	
Built in self test	



VLSI 82C325 Cache Controller

\* CACHE SUBSYSTEM CONTAINS SRAM AND BUFFERS

## **Personal Computer Design**

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**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80386DX

**System Bus:** AT

**Part:** VL82C335, TOPCAT DX Cache Controller

**Availability:** 1991

**Second Source:**

**Functions Contained:**

Supports 2-way set associative organization (32KB or 64KB)

Supports memory configurations up to 64MB

Fast look-aside architecture (cache & main accessed in parallel)

Programmable cache architecture (4 byte line size, 16 or 32 byte block size)

Write-thru memory update strategy

Least Recently Used (LRU) replacement algorithm

Write protect region support

Non-cacheable region support

Operates in Pipelined or Non-pipelined mode

Built in self test

Works in parallel with VL82C330

---

**Cache:** Yes

**Clock Speed:** 20, 25 & 33 MHz

**Main Memory Support:** No

**Schematic Not Available At Press Time**



**Manufacturer:** VLSI Technology, Inc  
**Processor Supported:** 80486 SX/DX  
**System Bus:** AT  
**Part:** VL82C486, Single-Chip Controller  
**Availability:** ?

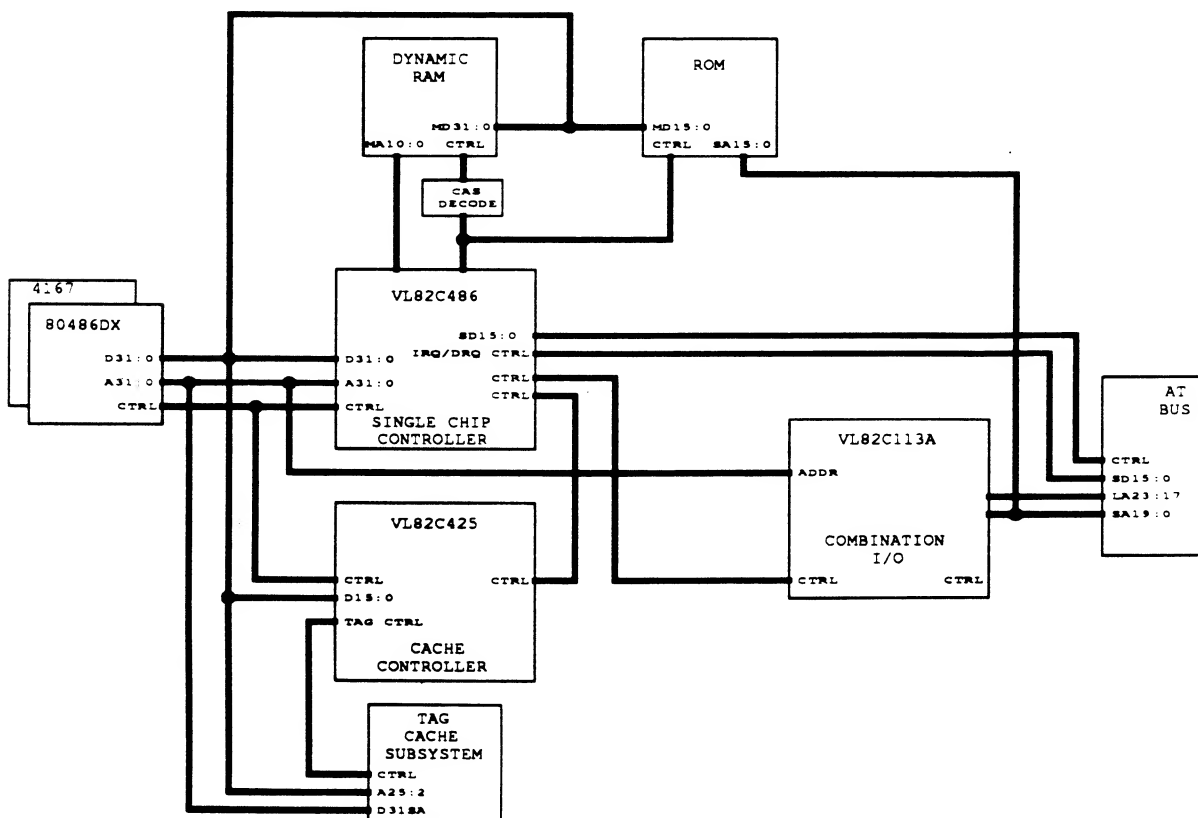
**Cache:** Yes  
**Clock Speed:** 33 MHz  
**Main Memory Support:** Yes

**Second Source:** ?

**Functions Contained:**

(two) 82C37A compatible DMA Controllers	(two) 82C59A compatible Interrupt Controllers
(one) 82C54 compatible timer/counter	74LS612 compatible Memory Mapper
(one) 82299 Bus Controller	Refresh logic (staggered RAS)
Port A, B, and NMI support	Parity generation
Supports up to 64MB memory (256K, 1M, or 4M DRAM)	Flash memory for BIOS ROM
page mode, 2/4 way interleave support	ROM chip select 8-bit or 16-bit ROM access
(one) 82284 compatible Clock Generator and Ready Interface	(one)

SCAMP = Single Chip AT Mid-range Performance



VLSI 82C486 PC/AT SYSTEM CONTROLLER  
 \* CACHE SUBSYSTEM CONTAINS  
 SRAM AND BUFFERS

## Personal Computer Design

**Manufacturer:** Manufacturer: VLSI Technology, Inc

**Cache:** No

**Processor Supported:** 80286, 80386SX

**Clock Speed:** 10-20 MHz (25 w/ System Bus)

386)

**System Bus:** AT

**Main Memory Support:** Yes

**Part:** VL82C310-FC VL82C311-FC, VL2C311L-FC - SCAMP-DT PC/AT System Controller

**Availability:** 1991

**Second Source:** ?

**Functions Contained:**

(two) 82C37A compatible DMA Controllers

(two) 82C59A compatible Interrupt Controllers

(one) 82C54 compatible timer/counter

(one) 82C288 compatible Bus Controller

(one) 74LS612 compatible Memory Mapper

(one) 82C284 compatible Clock generator and Ready Interface

Supports up to 8MB (VL82C311) or up to 16MB (VL82C310)

Peripheral controller

DRAM controller (2 way block interleaving)

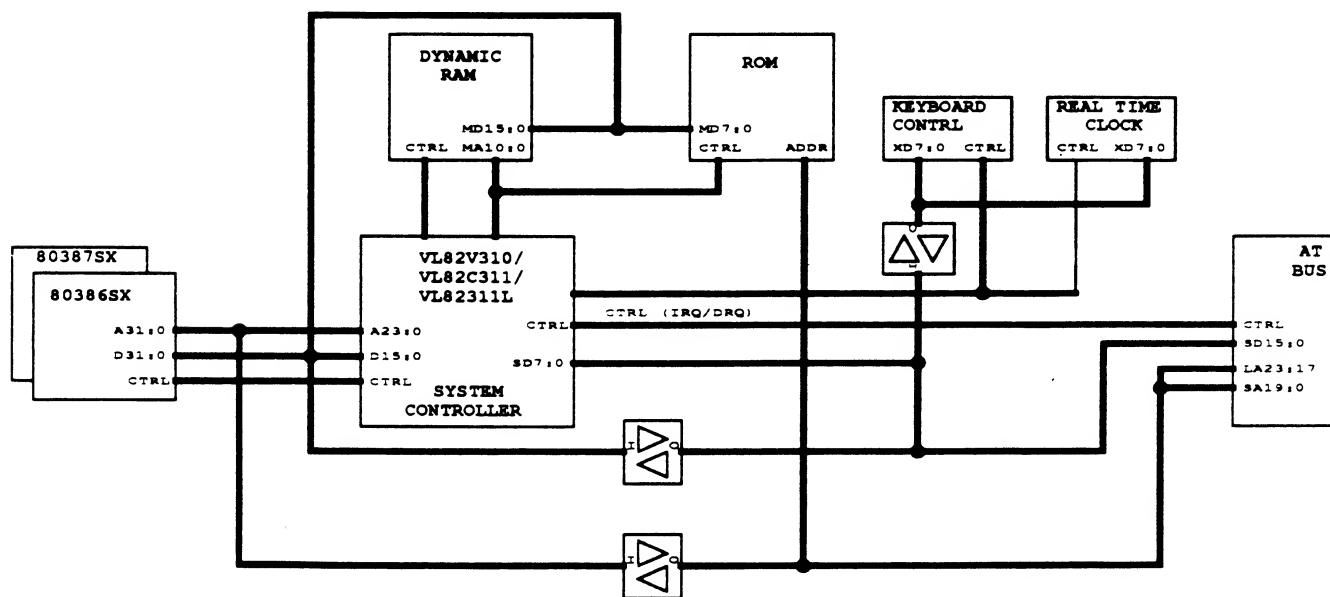
Address Controller

Supports system board refresh and timing of slot refresh

Supports LIM EMS 4.0

Shadow RAM supported (between 768K & 1M)

Supports 8-bit or 16-bit ROMs



VLSI VLC310/VLC311/VLC311L  
SCAMP PC/AT-Compatible System Controller

**Manufacturer:** VLSI

**Cache:** No

**Processor Supported:** 8088, 80286, 80386, 80486

**Clock Speed:** 3.1 MHz

**System Bus:** XT or AT

**Main Memory Support:** No

**Part:** VL16C450, VL82C50A, VL82C50 - Asynchronous Communications Element

**Availability:** ?

**Second Source:**

**Functions Contained:**

Full double buffering

Independent control of transmit, receive, line status and data set interrupts

Functionally compatible with standard 8250 & 16450 UARTs

---

Schematic Not Available At Press Time

## Personal Computer Design

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**Manufacturer:** VLSI

**Processor Supported:** 8088, 80286, 80386, 80486

**System Bus:** XT or AT

**Part:** VL16C451 & VL16C451B - Parallel/Asynchronous Communications Element

**Availability:** ?

**Second Source:** National Semiconductors NS16450 compatible

**Functions Contained:**

VL16450 with on-board Centronics printer interface

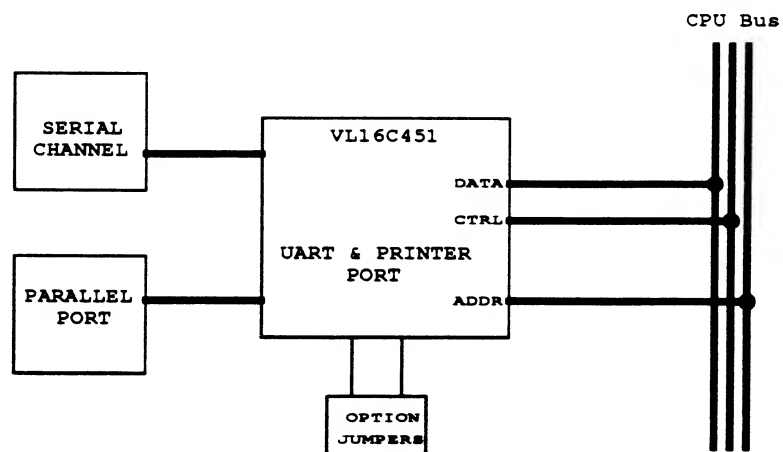
Enhanced bidirectional parallel data port (VL16C451B)

Crystal and oscillator clock inputs (VL16C451B)

General purpose input/output port (VL16C451B)

Tri-state control pin and in-circuit-test feature (VL16C451B)

---



VLSI 16C451 Asynchronous Communications Element With FIFO

**Manufacturer:** VLSI  
**Processor Supported:** 8088, 80286, 80386, 80486  
**System Bus:** XT or AT  
**Part:** VL16C452 & VL16C452B - Dual Asynchronous Communications Element  
**Cache:** No  
**Clock Speed:** 3.1 & 8 MHz  
**Main Memory Support:** No  
**Availability:** ?  
**Second Source:**  
**Functions Contained:**  
Bidirectional Centronics printer interface  
Programmable serial interface  
Tri-state indicator for COM1 to COM4 mapping of interrupts (VL16C452B)  
Buffered output for interrupt request signals on ISA bus

---

**Schematic Not Available At Press Time**

## Personal Computer Design

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**Manufacturer:** VLSI

**Processor Supported:** 8088, 80286, 80386, 80486

**System Bus:** XT or AT

**Part:** VL16C550, Asynchronous Communications Element with FIFO's

**Availability:** ?

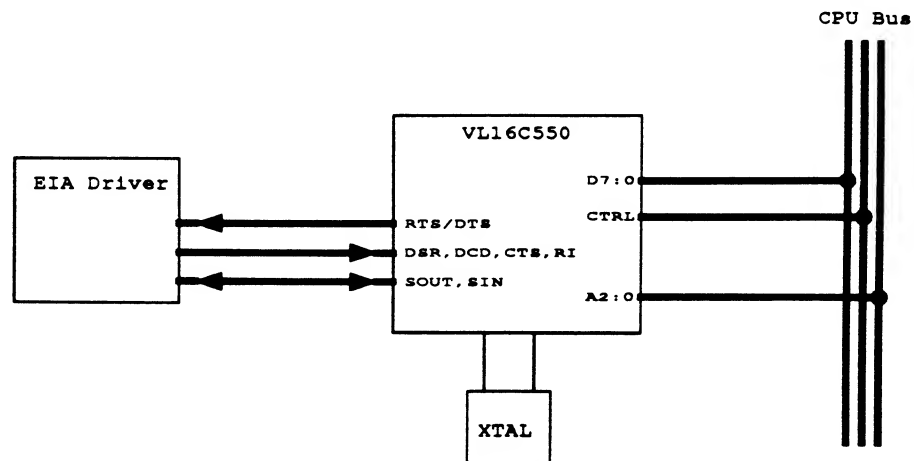
**Second Source:** compatible with VL16C450

**Functions Contained:**

(two) 16 byte First in First Out (FIFO) buffers

Independent control of transmit, receive, line status, data set interrupts and FIFOs

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VL51 16C550 Asynchronous Communications Element With FIFOs

**Manufacturer:** VLSI

**Cache:** No

**Processor Supported:** 8088, 80286, 80386, 80486

**Clock Speed:** 8 MHz

**System Bus:** XT or AT

**Main Memory Support:** No

**Part:** VL16C551, Asynchronous Communications Element with FIFO

**Availability:** ?

**Second Source:** compatible with VL16C451 and VL16C451B

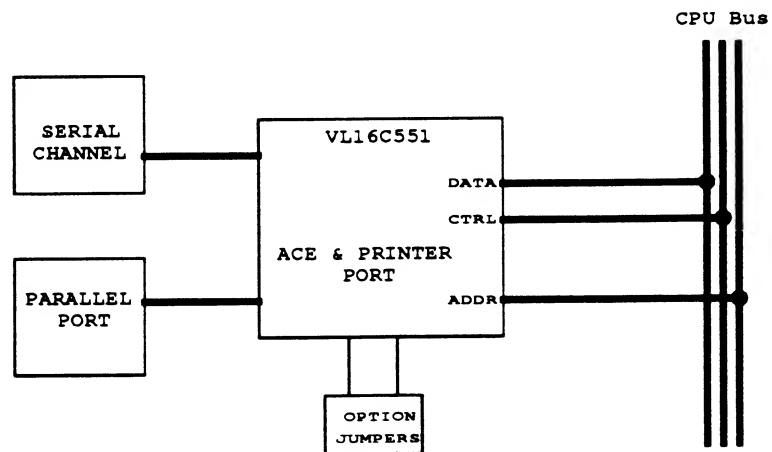
**Functions Contained:**

(two) 16 byte First in First Out (FIFO) buffers

Enhanced bidirectional line printer port

Independent control of transmit, receive, line status, data set interrupts and FIFOs

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VL51 16C551 Asynchronous Communications Element With FIFO

## Personal Computer Design

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**Manufacturer:** VLSI Technology, Inc

**Processor Supported:** 80386 SX/DX, 80486 SX/DX

**System Bus:** AT

**Part:** VL82C3216, Cache Controller and Write Buffer

**Availability:** ?

**Second Source:** ?

**Functions Contained:**

Supports up to 128KB

Supports independent programmable clock frequencies

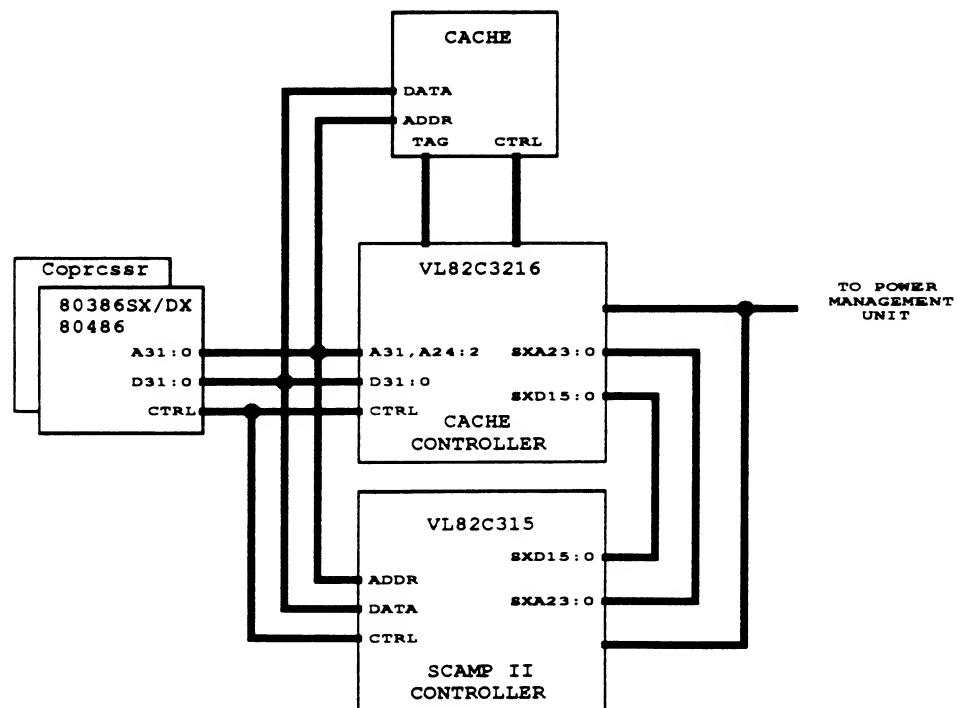
80486 internal cache control

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**Cache:** Yes

**Clock Speed:** 40 MHz

**Main Memory Support:** Yes



VL82C3216 Bus Expanding Controller (BANC) Cache With Buffer













# ***PC Design Guide***

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